

Design and Implementation of a Digital Phase Locked Loop for GPS Synchronization

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Abstract: In this paper, a Digital Phase-Locked Loop (DPLL) for GPS synchronization is designed, implemented and tested. It consists of a Phase Frequency Detector (PFD), an RC Low-Pass Filter (LPF), and a Relaxation Voltage Controlled Oscillator (VCO). The analysis, design, and examination of each block are carried out, resulting in a successful assembly of the entire DPLL circuit. The designed PLL is simulated, measured, and then compared with the experimental observations using LM565 IC. The findings demonstrate the PLL capability to achieve frequency synchronization with minimal phase error at the desired frequency of 1 KHz, along with a wide lock-in range.

Keywords: Digital Phase-Locked Loop, Phase Frequency Detector, RC Low-Pass Filter, Relaxation Voltage Controlled Oscillator.

1. INTRODUCTION

Synchronization is a vital process in any communication system, it refers to the action of aligning the frequency and timing of a communication system's components. Synchronization ensures reliable communication between a transmitter and a receiver and allows them to communicate in harmony by transmitting and receiving signals accurately without suffering from transmission problems such as data loss, signal distortion, higher bit error rates...etc [1-3]. Achieving synchronization in communication systems involves the use of a precise reference clock and different circuits such as phase-locked loops (PLLs). The reference clock aligns and coordinates the timing and frequency of the different components of the system. A common approach to obtain a precise clock is the use of GPS signals emitted by GPS satellites. The GPS satellites emit highly accurate 1PPS signals that are considered an available and reliable reference for synchronization purposes.

A PLL plays an important role in the process of synchronization [4-7]. It is a feedback control system that generates an output signal whose frequency is aligned with that of a reference signal, ensuring that both signals either maintain a constant phase difference or have no phase difference. This is achieved by continuously comparing the phase and frequency of the input signals and adjusting its local oscillator until the synchronization is

fulfilled. PLLs are of different types and are employed in a variety of applications [8-14].

In this work, a Digital PLL (DPLL) that synchronizes with a clock reference of 1 KHz frequency that achieves quite precision and stability is designed and implemented for GPS synchronization.

2. DESIGN AND SIMULATION OF A DPLL

In this section, the design and implementation of a DPLL for GPS synchronization is described. The main objective is to design a DPLL that synchronizes with a 1KHz reference signal. The design and implementation of the DPLL involve designing and simulating each block diagram in open loop, which means designing the Phase Frequency Detector (PFD), the Voltage Controlled Oscillator (VCO), and the Low-Pass Filter (LPF) separately and discussing their performance. Then, the closed loop DPLL system is constructed to study its behavior and to determine its ability to synchronize with the 1 KHz reference signal.

After conducting comprehensive testing on each individual block, the entire DPLL system is evaluated. This involved integrating the entire block, which includes the PFD connected to the LPF with specific resistor and capacitor values ($R = 1.28K\Omega$, $C = 200nF$), and further connected to the VCO. The circuit diagram of the implemented DPLL with the specified resistor and capacitor values is shown in Figure 1.

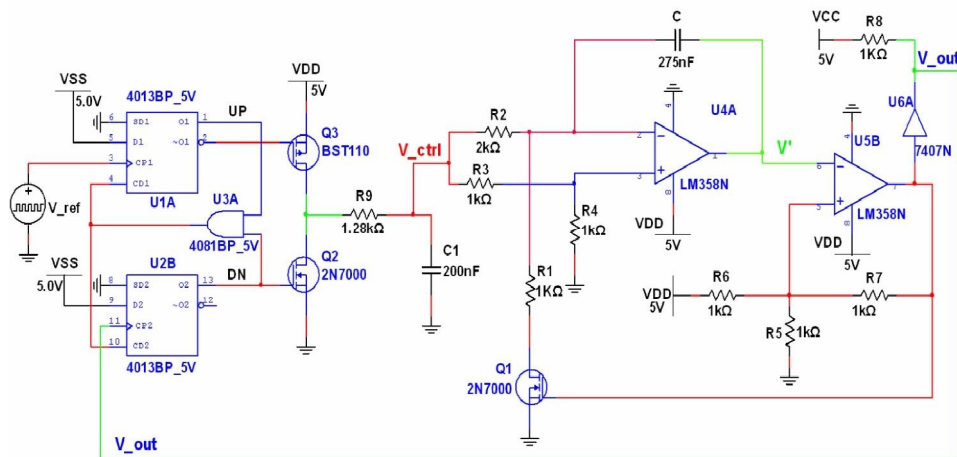


Fig. 1 Final schematic of the DPLL

The DPLL parameters such as Lock-in Range (LR), Settling Time (ST) and Power Consumption (PC) are simulated. By varying the input frequencies, it was possible to determine the lock-in range of the DPLL. The DPLL achieved phase lock at frequencies above 200 Hz, but it failed to maintain phase lock when the frequency is more than 1200 Hz. In terms of ST, the PLL takes 18 ms to lock at the reference frequency.

In order to determine the total consumed power, the power of each individual block was simulated, then the sum of the powers was calculated. Based on the simulation, the power consumption of the PFD is 9.60882 mW. The VCO consumes 4.753 mW of power, and the LPF has a power consumption of 9.390 mW. Therefore, the total power consumption is 23.75182 mW. Note that the PFD and the VCO are fed with 5 V power supplies, the voltage at the VCO input depends on the output of the LPF, it ranges from 0 to 5 V. The op-amps of the VCO have a power supply range of 3 V to 32 V when a single supply is used.

3. EXPERIMENTAL EVALUATION: RESULTS AND DISCUSSION

This section reports the experimental results of the DPLL and presents the interpretation and analysis of the findings. Based on the completed design of the DPLL and the circuit simulation in Multisim, the focus now shifts toward practical implementation. We present the implementation and the evaluation of the DPLL system including the circuit construction and essential measurements conducted on the output of its main blocks. We focused on

the frequency synchronization, the phase error, and the lock-in range. The PLL's performance will be compared with an IC PLL under similar conditions. The process of synchronizing the DPLL with the accurate 1PPS GPS signal, using a GPS module and GNSS software, will be performed.

In order to test the PLL shown in Figure 1, the circuit was constructed with the simulation values, but unfortunately the PLL did not meet the requirements. Moreover, the absence of some electronic components at the institute led to the reconstruction of the circuit with some modifications. The capacitors C and C1 were replaced by 330nF and 230nF, respectively. Regarding the resistor R9, 1.28 KΩ was the optimal value in simulation but not in practice, the PLL could not lock at 1 KHz using that resistance. Experiments showed that the RC filter resistor R9 should be replaced by 680 Ω. The PMOS and the NMOS transistors of the PFD were swapped by BS250 and BS170 respectively. The VCO was fed by +5V (including the LM358 op-amp, and the 7407N buffer), while the PFD was powered by +6.3V (including the 4013 D FF, the 4081 AND gate, and the BS250PMOS transistor). The voltage +6.3V was enough voltage to feed the three components at the same time, if 5 V is used instead, the output voltage at the LPF stage would be small, and thus the VCO will generate only lower frequencies. Another resistor of 1 KΩ was added between the Source of the BS250 PMOS and the +6.3 V power supply to limit the current flowing through the PMOS and to prevent it from damage since it handles a maximum current of 250 mA. The PFD and the DPLL circuits are shown in Figures 2 and 3.

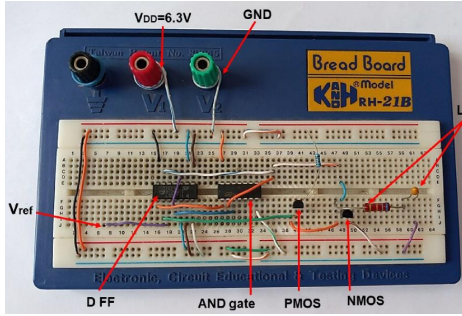


Fig. 2 Implementation of the PFD and the LPF circuit

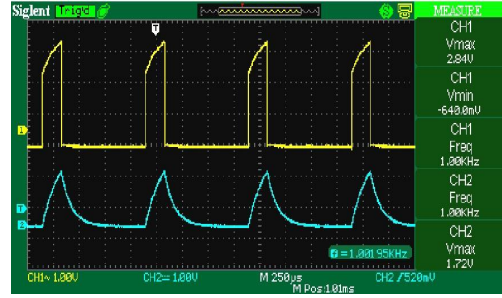


Fig. 5 PFD output (in yellow) and LPF output (in blue) at $f_{ref} = 1$ KHz

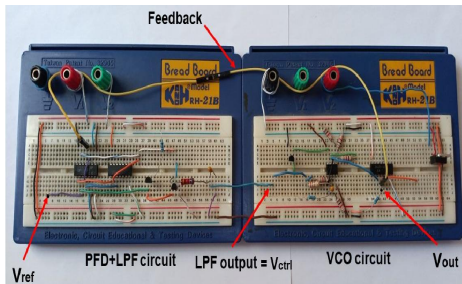


Fig. 3 Implementation of the DPLL circuit

Since the output lags the reference signal, DN signal is HIGH, it appeared as a train of narrow pulses of width equal to the ϕ_{error} as it is illustrated in Figure 6. UP signal appeared as glitches and it remained zero.

After constructing the whole circuit, a 1 KHz square signal was generated by a function generator and fed to the input port of the PLL, this is the reference signal. The reference and the PLL output signal were displayed on the scope screen. The waveforms are depicted in Figure 4.

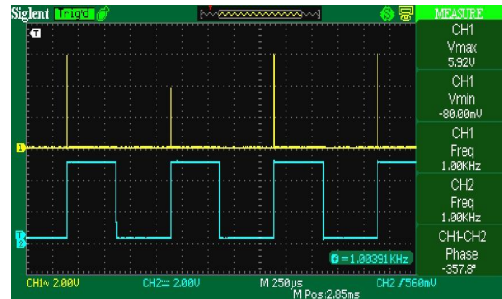


Fig. 6 DN signal (in yellow) and output signal (in blue) at $f_{ref} = 1$ KHz

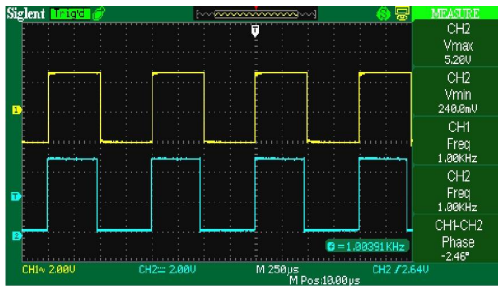


Fig. 4 Output signal (in blue) and 1 KHz reference (in yellow)

It is clear that the two signals are synchronized in frequency (1 KHz) with a small phase error of $\phi_{error} = -2.5^\circ$ as shown in the figure. Since ϕ_{error} is negative, this means that the output signal lags the reference signal with a short delay of $7 \mu s$. This phase error remains constant as the PLL continuously compares the two signals. The PFD and the LPF output signals are depicted in Figure 5. Note that the LPF output signal is an exponentially increasing and decaying signal due to the use of an RC filter.

We tested the PLL for different frequency input signals, the PLL generated an output signal that is frequency synchronized over a range that starts from 100 Hz to 1.6 KHz, but with different phase errors. The error was small in the neighborhood of the central frequency 1 KHz. Table 1 summarizes the phase error ϕ_{error} (in degrees) obtained at each frequency, note that the PLL maintains the error and keeps tracking the input signal.

The measurements show that the phase error is small when the frequency is close to 1 KHz, but as we move further away from it, the error gets increased but remains constant at each frequency.

After testing the PLL locking for various input frequencies and recording the phase error for each frequency, the next step was to compare it with a commercial PLL IC, specifically the LM565.

Table 1 Measurements of the phase error using the DPLL

f(Hz)	$\Phi_{error}(^\circ)$	f(Hz)	$\Phi_{error}(^\circ)$
1280	48.74	1020	9.12
1250	42.17	1010	3.2
1210	36.37	1000	-2.46

1180	29.3	990	-7.99
1150	26.24	976	-10.82
1130	22.38	934.5	-13.46
1110	20.3	877.8	-26
1090	18.34	870.7	-27.59
1080	15.79	863.5	-29.84
1070	14.11	856.1	-31.44
1060	14.41	842.6	-35.07
1050	12.9	828.9	-39.27
1040	11.57	809.3	-44.87
1030	11.03	796.9	-48.87

4. PLL PERFORMANCE COMPARISON: IMPLEMENTED PLL VS LM565

The LM565 is a commercial integrated circuit that serves as a general-purpose phase-locked loop. The LM565 is a 14-pin-out IC and it includes a PD, an amplifier, a fixed resistor for filtering, and a linear VCO. This IC is equipped with a stable and highly linear voltage-controlled oscillator and it's widely used in synchronization, FM demodulation, FSK demodulation...etc. The availability of this IC allowed us to conduct the comparison. The parameters of interest are the free running frequency f_0 , the loop gain K_0K_D , the natural frequency f_n , and the damping factor ζ . They are approximated by the following equations:

$$f_0 = \frac{0.3}{R_1 C_1} \tag{1}$$

$$K_0 K_D = \frac{33.6 f_0}{V_{CC} - V_{EE}} \tag{2}$$

$$f_n = \frac{1}{2\pi} \sqrt{\frac{K_0 K_D}{R_1 C_1}} \tag{3}$$

$$\zeta = \frac{1}{2} \sqrt{\frac{1}{K_0 K_D R_1 C_1}} \tag{4}$$

The free running frequency f_0 was set to 1KHz, and the difference $V_{CC}-V_{EE}$ was selected to be 12V. Then, the gain and the time constant were obtained,

$$K_0 K_D = 2800 \text{ and } R_1 C_1 = 0.3 \text{ ms}$$

If $R_1=3 \text{ K}\Omega$, then $C_1=0.1 \mu\text{F}$, and for a damping factor ζ of 0.5, the capacitor C_2 of the RC filter is equal to $0.1 \mu\text{F}$. The PLL was constructed using these components and tested with a 1KHz input signal from a function generator. The results recorded in Table 2 show the phase error for each input frequency.

This PLL locks starting from 330 Hz to 1040 Hz. Outside these boundaries, the PLL cannot acquire the lock. Measurements revealed that as we deviated from the 934.5 Hz frequency and approached 300 Hz, the phase error increased; however, it remained constant at each input frequency. For the desired frequency 1 KHz and its neighborhood, the IC worked perfectly, both input and output signals are phase and frequency synchronized. If the frequency exceeds

1.05KHz, the synchronization is no longer achieved.

Table 2 Measurements of the Phase error using LM565 PLL

f(Hz)	$\Phi_{\text{error}}(^{\circ})$	f(Hz)	$\Phi_{\text{error}}(^{\circ})$
790.3	-49.62	934.5	0
808.8	-41.94	976	0
828.9	-31.61	990	0
842.6	-33.83	1000	0
855.5	-19.96	1010	0
842.6	-33.83	1000	0
855.5	-19.96	1010	0
877.1	-17.68	1020	0
893.5	-8.62	1030	0
900.9	-4.54	1040	0
909.4	-5.76	1050	No locking

The results presented in Tables 1 and 2 demonstrate that in the neighborhood of the central frequency, the IC PLL performs exceptionally well, which aligns with expectations. In contrast, the proposed PLL achieves frequency synchronization within this range while maintaining a consistently small phase error. Moreover, the lock-in range of the designed PLL is wider than that of LM565 since it tracks the input signals of frequency up to 1.6 KHz. These results indicate that with further enhancements, the DPLL has the potential to replace the LM565 PLL in practical applications.

5. EXTERNAL HARDWARE-BASED 1PPS SIGNAL USE

In order to evaluate more the DPLL performance, the reference signal generated by a voltage source is replaced by the 1PPS signal generated by a real GPS receiver, namely NEO-M8N GPS module [15]. This module is highly capable and widely used GPS receiver module that offers accurate positioning and timing capabilities. This module provides a range of features and interfaces for seamless integration into various applications. One notable feature is the ability to provide a stable and accurate 1PPS signal, making it ideal for synchronization purposes. This module is connected to an external GPS antenna that captures signals transmitted by satellites as shown in Figure 7.



Fig. 7 External GPS antenna

The "1PPS" signal is a timing signal whose rising or falling edge occurs once every second, this signal serves as a reliable and precise reference point. It is commonly used in applications that require precise timekeeping and synchronization such as in Telecommunications, network synchronization, and navigation systems.

The 1PPS signal is generated by satellites, which are part of the global positioning system (GPS). They transmit precise timing information to the GPS receivers on the ground, along with positioning data (latitude, longitude, and altitude) that are widely used in navigation and mapping. Therefore, receivers derive the 1PPS signal from the satellite's signal.

According to the datasheet of NEO-M8N [15], a total of 24 pins are available, each serving a unique purpose. Among them, three pins are particularly noteworthy. Pin 24 is designated as the GND, pin 23 serves as the input power supply Vcc while pin 3 is specifically assigned as the TIMEPULSE pin, from which the desired 1PPS signal is obtained.

To interact with the NEO-M8N GPS module and make use of all of its features, the software U-center from U-blox manufacturer was utilized [16]. This software is designed for evaluating and analyzing global navigation satellite system (GNSS) data. It is used to process and interpret the data received from GNSS receivers, such as NEO-M8N module. The interface of U-center software is shown in Figure 8.

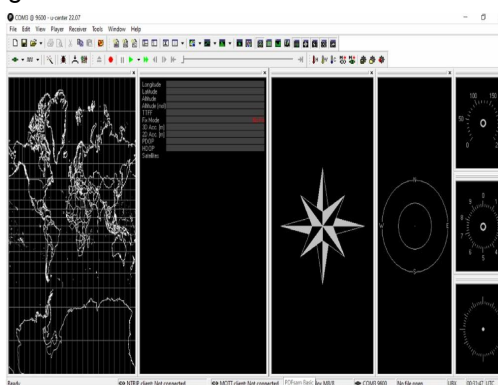


Fig. 8 U-center interface

To establish the connection between the GPS module and the software, the CH340 module is employed [17]. This module is responsible for converting the TTL-level signals from the GPS module into USB-compatible signals. It acts as an interface between the TTL-level signals from the GPS receiver and the USB port of the computer. The conversion is required since USB is typically used as a

standard communication interface by computers and the majority of today's devices. Overall, the combination of the NEO-M8N GPS module, the external antenna, the CH340 USB to TTL Converter Module, and the U-center software allowed us to effectively utilize the accurate 1PPS signal generated by the GPS module.

It is important to mention that one of the advantages of using U-center is that we can configure the behavior of the 1PPS signal by adjusting the TIMEPULSE parameters such as Time pulse Rate (frequency) and the Time pulse Length (duty cycle). Since the designed DLL synchronizes at 1 KHz, the 1PPS frequency was modified to 1 KHz with a duty cycle of 50%, that is a Time pulse Length of 0.5 ms. This signal was then introduced to the input of the PLL, and the phase error was measured following the same procedure as before.

The 1PPS signal is shown in Figure 9, it's a train of pulses of 100 ms width, 1 Hz frequency, minimum voltage of 160 mV, and a maximum pulse voltage of 3.60 V.

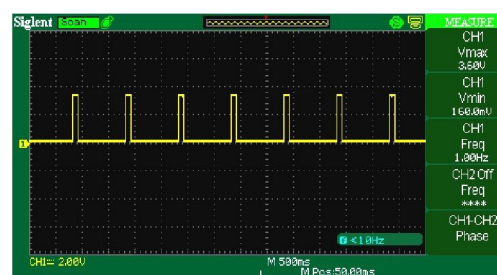


Fig. 9 1PPS GPS signal received by NEO-M8N

The 1 KHz reference signal was displayed using an oscilloscope as depicted below.

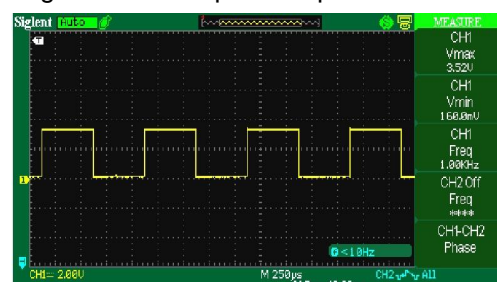


Fig. 10 1PPS GPS signal configured as reference of $f = 1$ KHz and $D = 50\%$

By inputting this signal to the DLL, the latter generated a signal whose frequency is equal to 1 KHz with a small error $\phi_{error} = -2.88^\circ$ which means that the output leads the reference by $8 \mu s$.

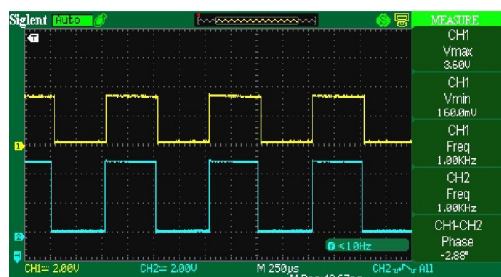


Fig. 11 PLL Output signal (in blue) and the GPS reference signal (in yellow).

The DPLL was tested for different input frequency signals, and the phase error was recorded for each frequency as shown in Table 3. These results are close to those of Table 1.

Table 3: Measurements of the Phase error using the 1PPS as a reference signal.

f(Hz)	$\phi_{\text{error}}(^{\circ})$	f(Hz)	$\phi_{\text{error}}(^{\circ})$
700.2	-81.08	950.5	-10.06
730.1	-69.81	970.5	-11.46
750.3	-62.7	980.3	-10.79
790.1	-49.38	1000	-2.88
800.2	-45.86	1100	20.92
820.2	-39.69	1200	36.7
850.3	-31.35	1300	55.82
890.3	-21.28	1400	79.51
900.5	-19.19	1500	110.6
930	-12.59	1600	183.9

It is concluded that the phase error is small when examining frequencies close to 1 KHz, but it progressively grows (either positively or negatively) as we move further away from that frequency.

6. CONCLUSION

In this paper, implementation and evaluation of a DPLL system has been presented. The DPLL blocks (PFD, LPF, and VCO) have been successfully implemented and tested, leading to the complete implementation of the PLL. The performance of the PLL, regarding the frequency synchronization and the lock-in range, has been assessed using a reference signal generated by a function generator and using an actual reference signal obtained from GPS satellites, specifically the 1PPS signal. The results demonstrated the successful synchronization of the PLL at the desired frequency of 1 KHz, validating its functional performance. Furthermore, a comparative analysis has been conducted between the implemented PLL and the IC PLL LM565. The outcomes revealed the synchronization capabilities of the DPLL with minimal phase

error at the desired frequency of 1 KHz, along with a wide lock-in range.

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