History of the Electrical Characterization and Test Platform Development at Microelectronics and Nanotechnology Division of CDTA, Algeria

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Abstract: The sixties (60s) and seventies (70s) of the last century have seen the takeoff of microelectronics. Since that, several countries, including Algeria, have adopted planned strategic programs to develop their domestic electronics. In this paper, we provide a historical review of the evolution of the electrical test benches developed at the Division of Microelectronics and Nanotechnology (DMN) of the "Centre de Développement des Technologies Avancées" (CDTA) or Center for Development of the Advanced Technologies. Starting from mid- nineties to up today, the electrical characterization platform has known different generations of test benches; from a simple setup to extract current-voltage (I-V) and capacitance-voltage (C-V) characteristics of semiconductor devices to more sophisticated ones to extract spectra of electrically detected magnetic resonance (EDMR). In addition, some benches have been developed to study reliability issue in metal oxide semiconductor (MOS) devices and integrated circuits (ICs), such as ionizing radiation effects, Fowler-Nordheim (FN) stress, hot-carrier injection (HCI), time-dependent dielectric breakdown (TDDB), and bias temperature instability (BTI). The obtained results have been published in well-known journals of the Institute of Electrical and Electronics Engineers (IEEE), the American Institute of Physics (AIP), and the Elsevier publishers.

Keywords: Electrical characterization, experimental setups, Device reliability test

1. INTRODUCTION

The semiconductor industry has been one of the most important industries in the world. It becomes a key driver of economic growth, innovation, and development of countries. This thanks to the revolutionary inventions of transistor, planar technology, and Integrated Circuits (ICs) **[1]**. After that, many important technological process developments happened to overcome numerous challenges toward improved transistors and IC. These developments marked the beginning of the microelectronics manufacturing story, which tremendously impacted the society life style and the world economy. It is characterized by rapid growth and technological innovations **[2].** Willing taking benefit of this emerging technology, several countries and governments have, since early 70s, targeted semiconductor manufacturing industry as strategic sector of development and supported it through various policies.

Among these countries, Algeria has heavily invested in electronics industry, like "Entreprise Nationale de l'Industrie Electronique (ENIE)" (ex SONELEC), which is a national company developed in collaboration with American industrial companies. At the same time, due to lack of qualified workforce of engineers and experts, Algeria built also "Institut National d'ELECtronique et d'ELECtrique (INELEC institute)" in collaboration with American universities to meet the American standards of educational trainings of engineers and technicians in electricity and electronics fields **[3,4]**. Discussions started in 1974 with University of Houston (College of technology), Oklahoma state university, and Wentworth institute of technology (Boston) for the Technology side; Case-Western University (Case institute, Cleveland), University of Missouri (Rolla), and Stevens Institute of Technology for the Engineering side; University of Wisconsin (Stout) for the design of the library; and General Telephone and Electric, Sylvania (GTE-Sylvania) company; Harris Corporation; and Raytheon for the industrial side. All these institutions were coordinated by Education Development Center (EDC) of Boston. The contract on the building, the equipment and the technical assistance was signed in 1976 with EDC and the first students in technology and electrical and electronics engineering were recruited at this date **[3, 4]**. The institute was, among other things, equipped with electrical testing instruments for semiconductor devices.

In fact, Algeria has deployed intense and varied efforts to bring in the semiconductors technologies of the northern industrialized countries to bridge the economic gap and emancipate the society. However, these efforts were not sufficient to make know-how transfer, because sustainable development requires continuous increase of skills and innovative capacities to attract modern technologies, absorb them, and transform them into new products. To reinforce and support the research and development (R&D) in electronics-based innovations, the microelectronics laboratory

was created at the “Centre de Développement des Technologies Avancées” (CDTA) in 1988. Later, the laboratory became Division of Microelectronics and Nanotechnology (DMN). Based on electronic design automation (EDA), technology computer-aided design (TCAD) tools, and electrical test instruments, the DMN has conducted R&D activities on IC designs; modeling/simulation of semiconductor devices and Micro-Electro-Mechanical System (MEMS) components; electrical characterization and reliability of semiconductor devices. The CDTA has become the focal point of microelectronics in Algeria.

It is well known that chip manufacturing process involves several steps. The main ones are chip circuit design, chip fabrication on silicon wafer, chip dicing/packaging, and chip electrical testing for quality assurance. The last step (electrical characterization) is crucial and performed during semiconductor device fabrication and it is carried out using testing equipment called a wafer prober and other test instruments. Furthermore, the customer requires precise device electrical characteristics and accurate measurements to detect any potential defects and ensure wafer quality. In this paper, we mainly focus on the electrical testing and device characterization. In fact, the point is not to present all the phases of the chip manufacturing process, but rather to relate our experience concerning one part of the process in order to inspire young researchers and urge them to persevere in providing much more efforts to succeed.

Historically, the chip electrical tests in Algeria date back to the end of 1970s at ENIE, national semiconductor Manufacturing Company to verify all functions of IC components during silicon fabrication and to manage silicon process variations and yield enhancement. In 1980s, INELEC was equipped with electrical test equipment of semiconductor devices and ICs for research/development purposes, where some results were published in scientific journals **[5-7].** Besides to already existing research activities on IC design, CAD tools **[8-16],** and device modeling/simulation **[17-25]**, the microelectronics laboratory of CDTA launched the activities on electrical tests and device characterizations in 1997 using Keithley electrometer and function generator instruments and Karl-Süss prober **[26-31]**. By upgrading its electrical test equipment, the DMN performed experimental works on reliability issues in semiconductor devices using Agilent instruments and semi-automated Cascade probe station **[32-38]**. Since that, several generations of in-house automated electrical test benches, illustrated in **Fig. 1**, have been developed for different research purposes **[39-48].** These homemade test solutions were cost-effective and allowed future expansions. The story of electrical test of semiconductor devices on wafer at CDTA reveals the transformation over the last thirty years of a team, of its characterization laboratory, and also of its working methods and communication. This electrical test platform development is mainly motivated by the need of CDTA Clean-Room Facility to evaluate its product reliability, i.e. estimation of the lifetime of the devices and circuits. In addition, what we also see emerging throughout this developments is, above all, the taste for experimentation and hands-on work within a platform equipped with testing instruments offering electrical test benches to young scientists

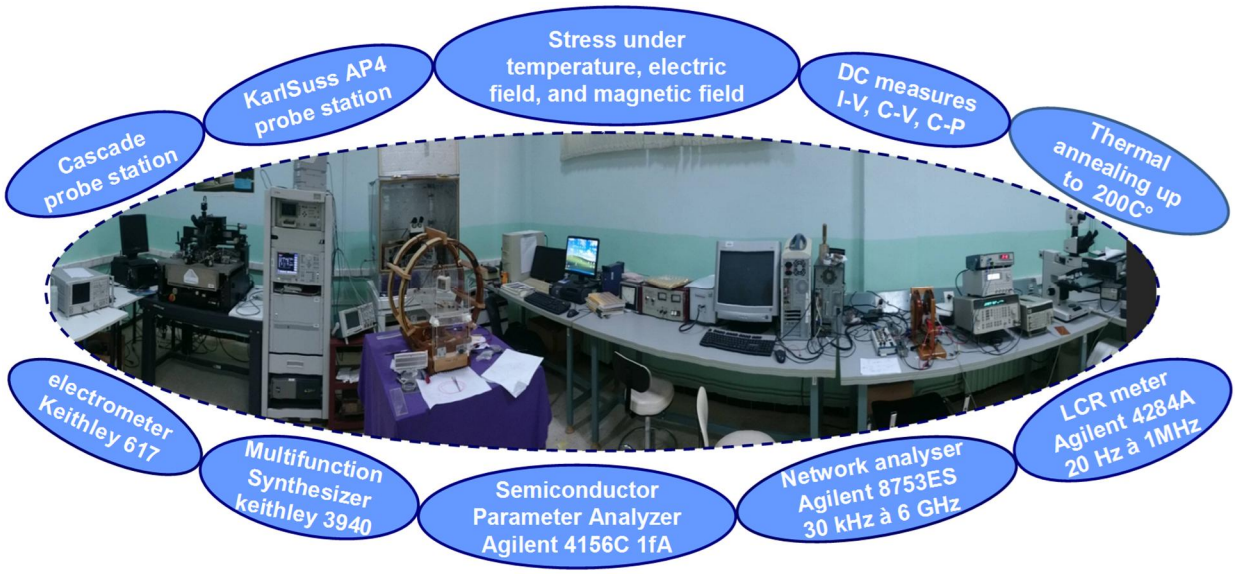

Fig. 1. Global view of the electrical characterization platform, showing reliability test setups for circuits and semiconductor devices.

and PhD students to innovate and demonstrate their creativity.

This review is intended for readers interested in the electrical test platform developments. It also provides researchers and engineers with information about the current experimental setups and potential capabilities of test benches at DMN/CDTA. The paper is organized as follows. Section II gives different electrical characterization setup generations developed at DMN/CDTA during the decade 1995-2005. These setups have been used to study the ionizing radiation effects in MOS devices. In addition, we describe test bench developed at INELEC before 1995. Test bench generations of the decade 2005-2015 are presented in section III. They serve to characterize Radio Frequency (RF) ICs, MEMS devices, to measure I-V/C-V on wafer level, and to investigate negative bias temperature instability (NBTI) in MOS transistors. The magnetic field and fast measurement test benches, introduced during the decade 2015-2025, are explained in section IV. The former has enabled EDMR spectra and magnetic capacitance extraction and the latter has allowed fast switching trap characterization. Section V synthesizes the evolution of the electrical characterization platform at DMN/CDTA. Concluding remarks are summarized in section VI.

2. PERIOD 1995-2005

Before 1995, the scientific activities at microelectronics laboratory of CDTA were limited to ICs design of digital/analog circuits, development of CAD tools for ICs design **[8-16]** and process/device modeling/simulation **[17-25]**. However, probe testing and chip characterization experiments were carried out at INELEC. In fact, Mitra and his team used Karl-Süss AP4 probe station of CDTA to perform device electrical characterization experiments. Their investigations were axed on surface states in MOS devices. They studied the charge and discharge of interface trap under non-steady-state emission using charge-extraction technique setup, given in **Fig. 2 [5-7]**. The test devices, which are MOS capacitors and MOS field effect transistors (MOSFETs), were designed at microelectronics laboratory of CDTA and fabricated at European Silicon Structures (ES2), France using 2-µm complementary MOS (CMOS) process. The p-well has a doping concentration of 7.6×10^{15} cm^{-3} for all used pMOSFETs. The common n-substrate, having a doping concentration of 2.7×10^{16} cm^{-3}, is used for MOS capacitors. Dry nitrogen annealed oxide is used for all devices which has a thickness of 400Å.

The test devices were mounted within a test-fixture HP 16055 or within Karl-Süss probe station depending on packaged or non-packaged devices, respectively. The experimental setup of the implemented technique is illustrated in **Fig. 2**. The desired voltage signal in the form of a square wave is applied on the gate MOS device using the function-generator, Wavetek 180 coupled with the programmable dc substrate current. The frequency of the gate voltage was measured by the HP 5384A frequency counter and its amplitude by the HP 3478A multi-meter. Software was developed so that the HP 9836 computer may read and control data from different meters and process them to give the required dc substrate current versus gate voltage and frequency curves.

The technique uses the substrate current arising from the non-steady-state emission of carriers from the surface states instead of that arising from their steady-state recombination as in the charge pumping (CP) technique **[49]**, while the gate signal amplitude is confined between threshold and flatband voltages in such a way that the surface region of the device does not cross the depletion limits and the surface potential remains always under the depletion conditions **[6, 7]**.

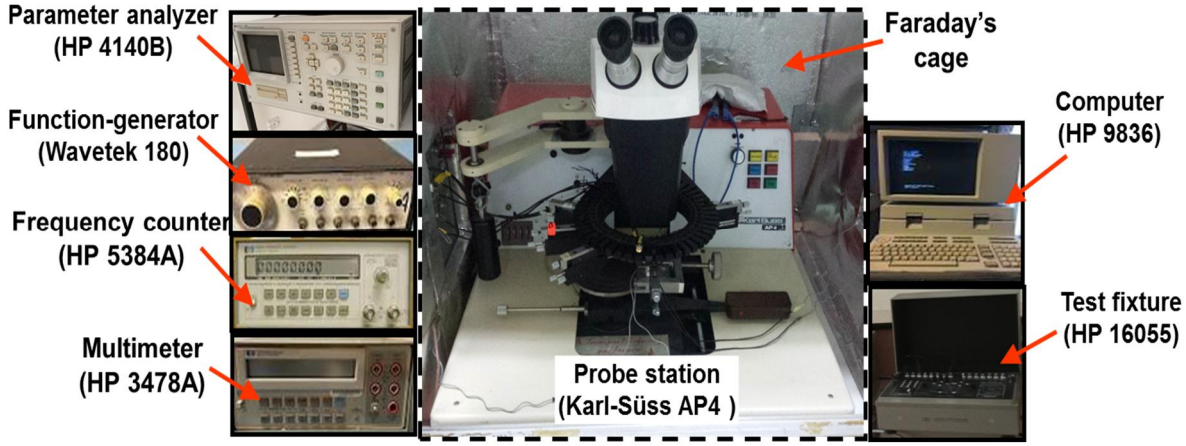

Fig. 2. Experimental Setup of INELEC, showing Karl-Süss probe station and instruments used to characterize MOS devices.

Figure 3 shows the net substrate current measured under non-steady-state emission conditions for different gate areas of MOSFET devices (a: 300×8, b: 80×20, and c: 80×8 µm^2). The experiment has been also repeated by using MOS capacitors, which give similar results **[7]**. This fact implies that a net charge passes from the gate to the substrate through the oxide to fill the empty surface states at the Si/SiO_2 interface during one half of the gate voltage swing, whereas the same surface states emit their electrons to the substrates during the other half. As this current extracts charge from the gate, so it is named charge extraction current (I_{ce}) in order to distinguish it from the CP current (I_{cp}) for which charge is pumped from the drain/source. The current as a function of frequency curves (I_{ce}-f) are well discussed and modeled in **[7].**

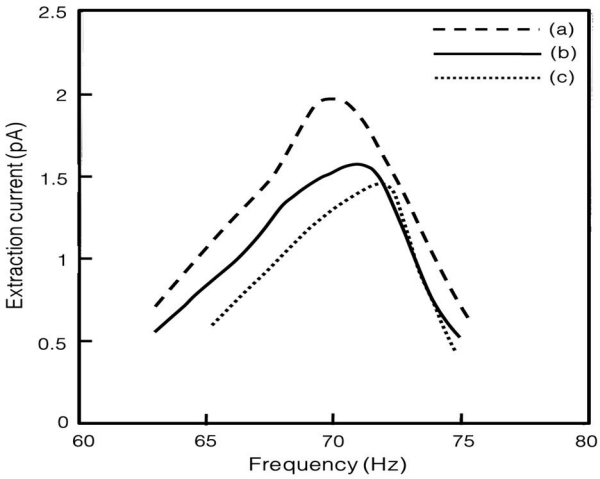

Fig. 3. Experimental I_{ce}-f curves for the surface-potential sweep from E_B to E_i for MOS transistors of different areas: **a:** 300X8, b: 80X20, and c: 80X8 µm^2 **[7]**. Reproduced with permission from Mitra *et al.*, IEEE Trans. Electron Devices 40(5), 923-931(1993). Copyright 1993 IEEE Publishing.

A. DMN/CDTA-Setup: Generation-1 (1997)

The microelectronics laboratory of CDTA built its first electrical characterization setup at CDTA on 1997 using function generator (Philips 5134), electrometer (Keithley 485), and oscilloscope (Tektronix 2201), as illustrated in **Fig.4**. This experimental bench was used to investigate the ionizing radiation effects in MOS devices **[26, 27]**. The irradiation was performed using gamma ray at CRS (Centre de radio-protection et de Sûreté) laboratory, Algeria.

To understand the ionizing radiation effects in MOS structures, such as mechanisms which govern the oxide trap and interface trap creation and their relation to the threshold voltage shift, characterizations were conducted before and after irradiations of MOSFETs by ^{60}Co Gamma rays source. The studied transistors were designed on test circuit at microelectronics laboratory, CDTA, and fabricated at ES2. The transistors were fabricated using CMOS, 2 µm, and dual metal technology on p-type silicon (100) substrate with normal concentration of 7.6 × 10^{15} boron/cm^3, 40 nm thick gate oxide (SiO_2) layer grown in dry O_2, and N^+_poly-silicon gate. The gate capacitance per area unit, C_{ox} is about of 8.6 × 10^{-8} (F.cm^{-2}). MOS devices were placed at 28 cm from the gamma

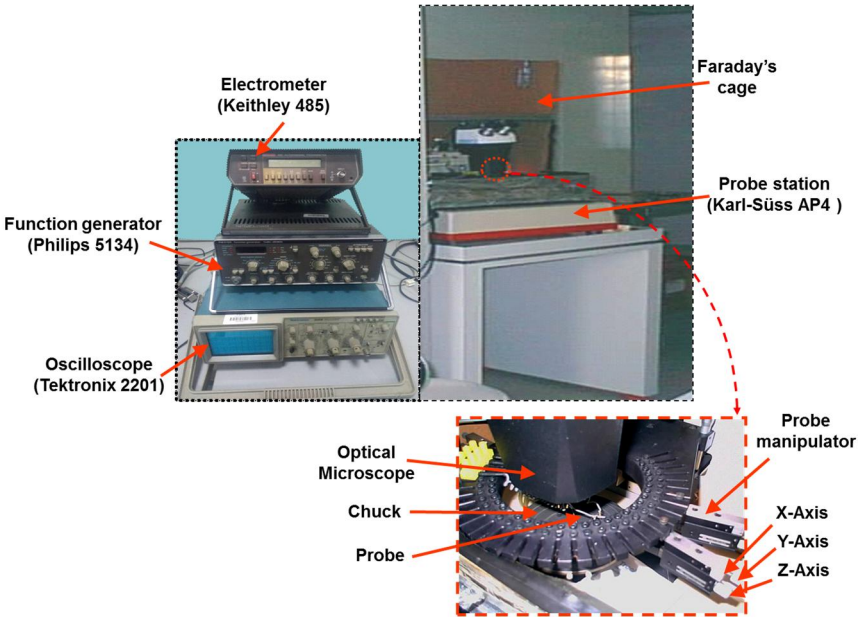

Fig. 4. Experimental Setup Setup_Generation-1 (1997), showing probe station and instruments used to characterize MOS devices.

source and irradiated at different low doses of 10, 50, 100, 150, 250 krad under zero bias at room temperature. The standard CP technique was utilized to characterize the devices before and after each irradiation. During characterization, the MOSFET source/drain terminals were grounded, the gate terminal was pulsed by applying a triangular pulse train with amplitude ΔV_G of various frequencies using the generator function, and the substrate terminal was grounded via the electrometer. The measurements were performed at room temperature using the sensitive Keithley 485 electrometer, the pulse generator, and the micro-manipulator probe station. The test circuit chip (non-packaged) within the probe station were isolated from vibration and enclosed in a grounded faraday box to avoid both RFI and light effects. Data were drawn via plotter table.

Figure 5 (a) gives the evolution of the radiation-induced threshold voltage shift (ΔV_{th}) with total radiation dose. ΔV_{th} exhibits a turn-around effect due to the contributions of two components **[26, 50]**. In fact, ΔV_{th} shift consists of interface trapped charge increase (ΔV_{it}) and oxide trapped charge buildup (ΔV_{ot}) caused by the irradiation [see **Fig.5 (a)**]. The growth of the interface charges ΔQ_{it} leads to a positive threshold voltage shift, $\Delta V_{it} = \Delta Q_{it}/C_{ox}$. On the other hand, the increase of the oxide charges ΔQ_{ot} leads to a negative threshold voltage shift, $\Delta V_{ot} = -\Delta Q_{ot}/C_{ox}$. We notice here that ΔV_{th} tends initially to negative voltage due to positive oxide charge build up at 10 krad, followed later by positive threshold voltage shifts at a total dose of 150 krad due to the increase of negative interface charge.

In **Fig. 5 (b)**, a comparison between radiation-induced ΔV_{th}, obtained from transistors of different channel lengths. It is clearly illustrated that threshold voltage shift curves have the same general feature and behavior for all degraded nMOS transistors. The results show a strong radiation-induced ΔV_{th} shift dependence on gate length. During irradiation, the threshold-voltage shift is more negative for transistors with shorter gate lengths than transistors with longer gate lengths **[27, 51]**. In addition, ΔV_{th} shift tends to positive direction with radiation dose increase. Thereby, we expect that, at high radiation dose, ΔV_{th} should be more positive for transistors with longer gate lengths than transistors with shorter gate lengths. By exploring the interface- and oxide-trap creation, a best understanding of the impact of the channel length on radiation-induced threshold voltage shift was achieved. Radiation-induced threshold voltage shift consists of two components

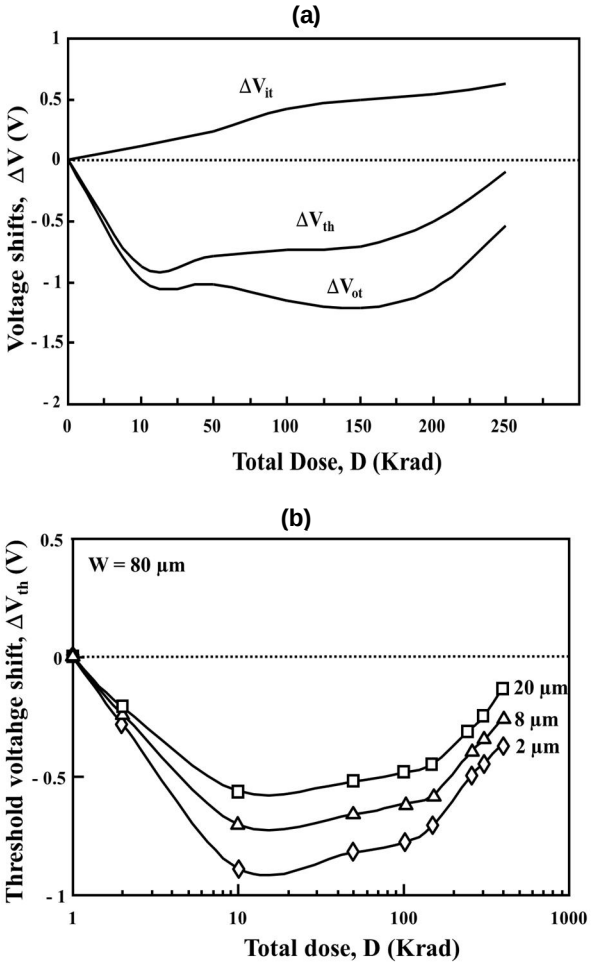

Fig. 5. (a) ΔV_{th} shift and its components ΔV_{it}, and ΔV_{ot} vs. total dose **[26]. (b)** Radiation-induced threshold-voltage shift as a function of total dose for nMOS transistors of different designed gate lengths **[27]. (a)** Reproduced with permission from Djezzar *et al.*, IEEE Trans. Nucl. Sci. 46(4), 829-833(1999). Copyright 1999 IEEE Publishing. **(b)** Reproduced with permission from Djezzar *et al.*, IEEE Trans. Nucl. Sci. 47(6), 1872-1878(2000). Copyright 2000 IEEE Publishing.

[50], a shift induced by the interface traps, ΔV_{it} and a shift induced by the oxide traps, ΔV_{ot}. It has been shown that ΔV_{it} remains approximately unchanged for all transistors, while ΔV_{ot} depends strongly on the gate length **[27]**. The origin of the oxide trap charge augmentation with decreasing the gate length is probably caused by total stress in the gate oxide, where a small gate length introduces a large compressive strain in the oxide **[52, 53]**. In fact, during the fabrication process, the gate oxide, especially the oxide near the gate edges, is susceptible to unintentional stress of process steps (ion implantation, etching ... etc.). Furthermore, the quality of the oxide near the gate edges is affected by mechanical strains caused by the discontinuity of the gate electrode. These different stresses increase with reducing the gate length.

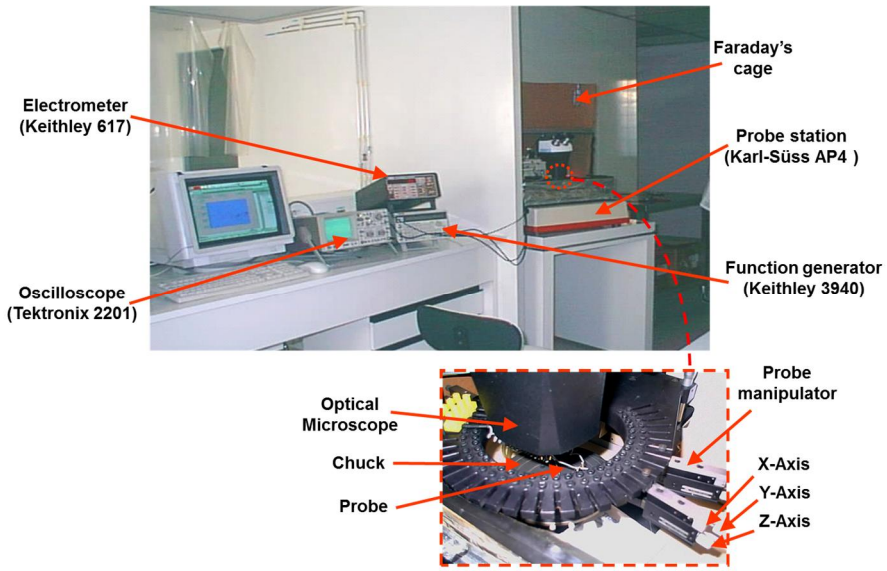

Fig. 6. Experimental Setup_Generation-2 (1999), illustrating prober and instruments used to extract I-V, C-V, and CP of MOS devices.

B. DMN/CDTA-Setup: Generation-2 (1999)

The experimental hard/soft setup was upgraded by acquiring LabVIEW software and new instruments namely a function generator (Keithley 3940 multifunction synthesizer) and an electrometer (Keithley 617) with programmable dc voltage supply allowing development of automated measurements. **Figure 6** shows instruments used for current-voltage (I-V) and charge pumping (CP) techniques and their variant methods. The instruments are connected through a general purpose interface bus (GPIB). All electrical test methods/techniques and data acquisition/treatment have been automated using computer and LabVIEW software **[54].** This automated electrical test environment facilitates reliable measurements, ensuring ease, and rapidity.

The setup of **Fig. 6** was used to study the near-interfacial oxide traps or border traps **[55, 56]** and their influence on the radiation response, and the long-term reliability of irradiated MOS devices. In this investigation, combined voltage CP (I_{CP}–V_L) (V_L is signal low level voltage) and frequency CP (Q_{CP}–f) techniques were used to investigate the generation and evolution of border-traps in irradiated nMOS transistors. Details of the experimental conditions have been previously described in the above section. Irradiation is performed up to 400 krad on non-packaged samples by using 1.25 MeV γ-rays at room temperature. The γ-ray was produced by ^{60}Co cell with low dose rate of 200 rad/min. I_{CP}–V_L and Q_{CP}–f measurements were made before and after each irradiation at 25 °C. We made a long delay between irradiation and measurements. I_{CP}–V_L standard curves (Elliot curves) were extracted using a triangular signal with amplitude of 3 V and frequency of 100 kHz. The technique consists of varying V_L from - 6 to 2 V. Q_{CP}–f curves were obtained by maintaining the signal position fixed (position where CP current is maximum, I_{CPmax}) and varying the frequency from 10^2 to 10^6 Hz.

Figure 7 summarizes the evolution of charge recombined per cycle versus frequency (Q_{CP}–f) curves in nMOS transistors with different gate lengths 2 µm (T1), 8 µm (T2), and 20 µm (T3) and fixed width of 80 µm for each step of irradiation at low frequencies **[28]**. The border-trap density (ΔN_{bt}: number of traps per area unit) is extracted from the inclination of Q_{CP}–f segment at low frequencies. We note here that ΔN_{bt} corresponds only to a fraction of the border-traps; the fastest border-traps that can exchange their charge with the substrate during the CP cycle **[57, 58]**. Nevertheless, this permits to estimate the relative importance of border-traps with respect to interface-traps in the electrical response of transistors.

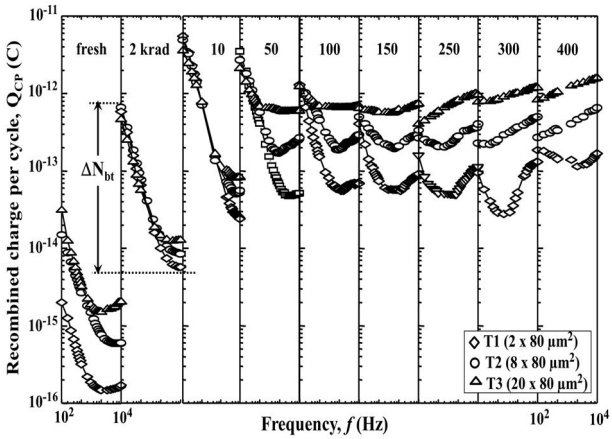

Fig. 7. Recombined charge pumping (Q_{CP}) versus frequency of irradiated nMOS transistors with different gate lengths for several total doses **[28].** Reproduced with permission from Djezzar *et al.*, Microelectron. Reliab. 42(12), 1865-1874 (2002). Copyright 2002 Elsevier Publishing.

The curves reveal two behavior types of the segment inclination with dose increase: initially, there is an augmentation, followed later by a decrease. This indicates that border-trap creation and annealing (or compensation) mechanisms take place at the same time. At low doses, the creation mechanism is dominant, while at high doses the second is important. This is probably due to low dose rate of radiation (200 rad/min). In other terms, because of the longer times associated with low dose rate irradiation, more annealing processes can occur. Djezzar et *al.* have previously discussed this behavior **[26].**

The investigation of the evolution of border-trap with gate length is illustrated in **Fig. 8 [30, 55]**. The results illustrate a strong radiation-induced border-trap shift dependence on gate length. After each irradiation, ΔN_{bt} is much more significant for transistors of shorter gate lengths than for transistors of longer gate lengths. This clearly indicates that transistor geometry can have a large effect on the density of active border-trap in a given device, perhaps because of differences in the near-interfacial stresses and near-channel-edge strains. We note here that the same effect of gate length has been reported for radiation-induced oxide traps **[27, 58]**. Transistors with shorter gate lengths present more much important trap density increase than transistors with longer gate lengths during irradiation. This similarity strengthens the correlation between border- and oxide-trap and reinforces the idea that both traps could have necessarily close microscopic structures. Whatever its structure, the border-trap must be taken into account for radiation response and long-term reliability of MOS devices in space applications,

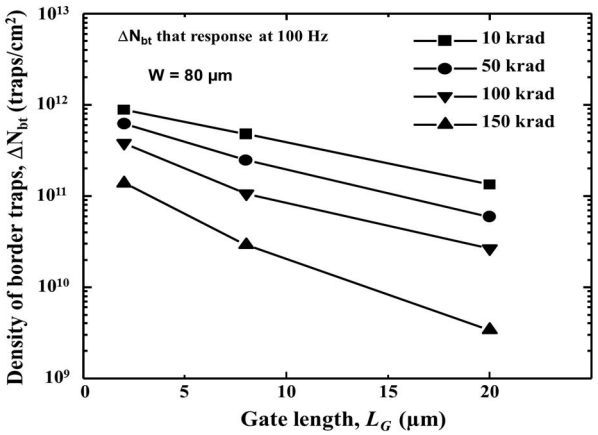

Fig. 8. Border-trap density versus designed gate length at 10, 50, 100, and 150 krad **[30].** Reproduced with permission from Djezzar *et al.*, IEEE Nuclear Science Symposium (NSS, IEEE, 2001), pp. 234-239 (2002). Copyright 2002 IEEE Publishing.

especially, in modern MOS device technology, where their thinner oxides may only contain the border-traps.

C. DMN/CDTA-Setup: Generation-3 (2003)

To keep going our mission, the infrastructure and electrical test equipment were extended in 2003 by getting raked-equipment solution, presented in **Fig. 9**. The rake includes parameter analyzer (Agilent 4156C), LCR meter (Agilent 4284A), switching matrix (Agilent E5250A), and generator expander (Agilent 41501B). This solution made it possible to deeply investigate the physical and failure analysis in materials and devices **[32-37, 60-65].** It also enabled the development of

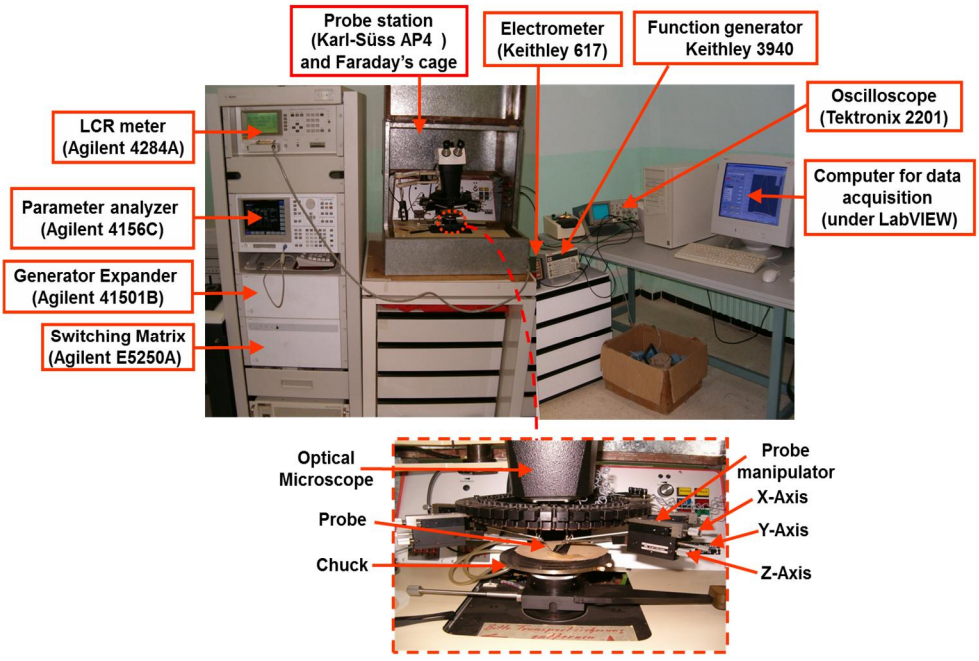

Fig. 9. Experimental Setup_Generation-3 (2003), showing probe station and Agilent instruments used to implement the OTCP method and characterize semiconductor devices.

electrical test methods that assist in identifying the contribution of different types of defects involved in MOS device degradation. This test bench allowed the implementation of the Oxide-Trap based on Charge-Pumping (OTCP) method at High-Frequency (HF-OTCP) **[32]** and low-Frequency (LF-OTCP) **[33]**. The OTCP extraction method permits to evaluate radiation-induced interface traps (ΔN_{it}), oxide traps (ΔN_{ot}), and border traps (ΔN_{bt}) in MOSFETs.

To validate the OTCP method, it was compared to several routinely methods, used to electrically sense different radiation-induced traps in oxide and at/or near interface of MOS devices **[35, 60, 61]**. The practical ones are midgap (MG) **[66],** subthreshold slope (STS) **[67]**, C-V **[68],** dual-transistor CP (DTCP) **[69]**, dual-transistor border trap (DTBT) **[70]** methods, giving a clear insight on the benefits and limitations of OTCP. The validation was performed on MOS devices (pMOSFET, nMOSFET, nMOS and pMOS capacitors) fabricated on the same chip at the Institute for Silicon Technology (ISiT) of Fraunhofer, Germany. The process is a dual-layer-metal 1-µm CMOS twin-well technology on p-type 12-µm epilayer on silicon 100 substrate with 20-nm-thick gate oxide layer grown in dry O_2. Cox is about 2.12×10^{-7} $F{\cdot}cm^{-2}$. The non-packaged transistors have a gate length ranging from 1 to 10 µm with fixed gate width at 10 µm.

Figure 10 shows ΔN_{ot} (a) and ΔN_{it} (b) extracted by STS, MG, DTCP, DTBT, and C-V normalized to those extracted by OTCP for nMOSFET and p-type MOS capacitor **[35]. Figure 10 (a)** shows that all ΔN_{ot} given by classical methods are obviously constant for each nMOS transistor gate width. They show 20%–50% variation from ΔN_{ot} of OTCP. Unlike ΔN_{ot}, ΔN_{it} shows a large dispersion, classical methods give values of ΔN_{it} more than three times higher than the value of ΔN_{it}-OTCP. The same as for oxide-trap density, the variation of interface-trap density given by all methods does not exceed an order of magnitude. On the one hand, the discrepancy between DTBT and the other methods is due to the fact that DTBT as well as OTCP extract and separate all kinds of traps, while the others do not, since they consider border traps like interface traps. On the other hand, one possible cause could be the difference in the definition of the band gap position which contributes in ΔN_{it}. DTCP and DTBT methods combine two techniques and must be applied to N- and P-channel transistors with identically oxides, irradiated under identical conditions, whereas OTCP uses a single transistor and a single technique. DTCP and DTBT give average densities for whole nMOS and pMOS devices. Moreover, border traps are taken as interface traps in the DTCP method and have an energetic distribution in the silicon band gap in DTBT method, while, in the OTCP method, they are considered like oxide traps. Furthermore, HF-OTCP method was used to explore the influence of

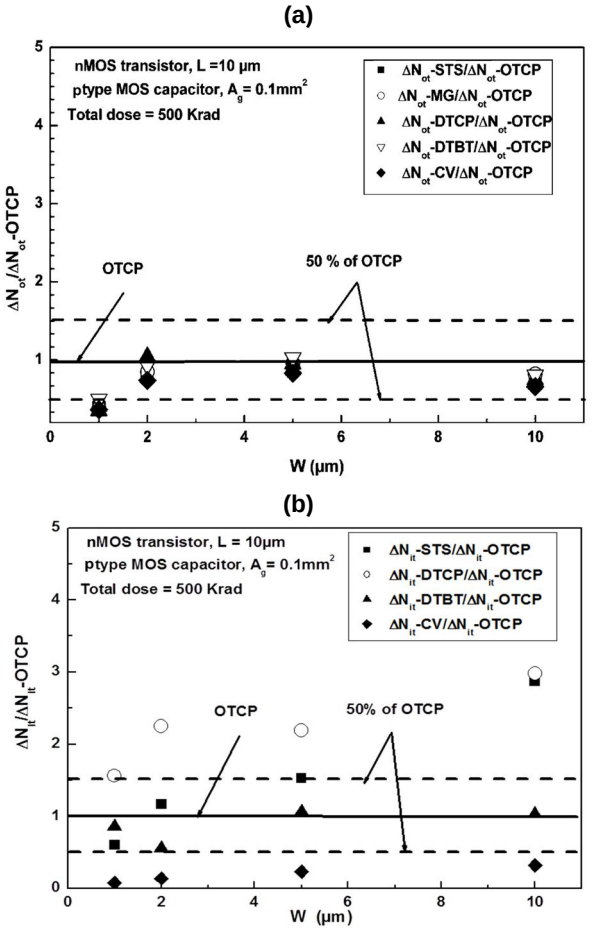

Fig. 10. (a) Radiation-induced oxide traps, ΔN_{ot} extracted using conventional methods; STS, MG, DTCP, DTBT, and C-V normalized to ΔN_{ot} determined by the OTCP method **(b)** Radiation-induced interface traps ΔNit extracted using STS, MG, DTCP, DTBT, and C-V normalized to ΔN_{it} determined by the OTCP method for nMOSFET and p-type MOS capacitor **[35].** Reproduced with permission from Djezzar *et al*., IEEE Trans. Device Mater. Reliab. 9(5), 222-230(2009). Copyright 2009 IEEE Publishing.

gate oxide thickness on traps created by radiations in two different transistors with gate oxides of 20 and 40 nm **[61].** We have found that the thinner is the oxide, the weaker is the degradation. This means that reducing gate oxide thickness implicates fewer problems with total ionizing dose effects in MOS devices.

In addition, by combining Silvaco simulations **[71]** and CP measurements, we were able to extract the contribution of different regions of MOSFET in CP measurements **[37, 38, 72, 73]**. This methodology allows to take out the lightly doped drain (LDD) subdiffusion and local oxidation of silicon (LOCOS) effects from CP curves, leaving only the CP current of the effective channel, in narrow- and short-channel MOSFET transistors **[37, 38, 72].** The contribution of LDD-subdiffusion and LOCOS regions to the CP characteristics was clarified by extracting the spatial distributions of

threshold and flatband voltages in gate area using Silvaco software. **Figure 11** shows the constant-amplitude CP measurements in the effective-channel, LDD-subdiffusion, and LOCOS regions. **Figure 11 (a)** shows the I_{CP}–V_L curve of the LDD-nMOSFET transistor with W_G/L_G = 10/1 in logarithmic scale, and **Fig. 11 (b)** shows the distributions of V_{th} and V_{fb} along the interface in the effective-channel, LDD-subdiffusion, and LOCOS regions. These distributions are obtained by Silvaco TCAD simulation for nMOS. To well illustrate the CP zone in **Fig. 11 (b)**, the V_{th} distribution is shifted downward by ΔV_G = 4 V. For specified V_L, the intersections of V_L line (see dashed lines) with V_{th} and V_{fb} curves define the area between V_{th} and V_{fb} curves, at which the total capture of both electrons and holes by traps occurs, and therefore define the CP current. The local variation of V_{th} and V_{fb} along the channel is due to the doping profile. However, the V_{th} and V_{fb} distributions along the interface under the LOCOS region are due to both nonuniform doping and oxide thickness of additional parasite transistors. According to the aforementioned CP scan, it is clear that the maximum current is affected by both LDD-subdiffusion and LOCOS-edge regions [see (C)]. It is also obviously apparent that the rise and fall edges of the CP curve are influenced by the LDD-subdiffusion and LOCOS-edge regions, respectively. From the above mentioned analysis, the contributing area to CP current changes with V_L variation in the constant-amplitude CP technique. While the rising of gate-pulse top (V_H) opens up additional regions for CP process, the rising gate-pulse bottom (V_L) ejects area from CP. To model the contributing area to CP current, we simulate the nMOSFET device.

Figure 12 gives Silvaco-based simulated I_{CP}–V_L curve with its model-based components and the experimental CP curve performed on LDD-nMOSFET with W_G/L_G = 10/1 **[73].** The curves are plotted in linear and logarithmic scale to illustrate the correlation. There is obviously a great similarity between the simulated total CP curve and the experiment data for all shaped parts. In addition, the contribution of different regions to the total I_{CP}–V_L characteristic is illustrated on the same figure. The rising edge of both experimental and total simulated I_{CP}–V_L characteristics presents two tails. The first tail is just under V_{th} of the effective channel and located in regions (B) and (C) [see **Fig. 12 (a)**]. The second tail is located in region (A) and extends from the end of the first tail deeply toward the negative bias. They are mainly caused by nonuniformity of doping distribution across Channel-Eff/LDD-Sub and LDD regions, respectively. The first tail only occurs in I_{CP}–V_L of the LDD devices and has no equivalent in I_{CP}–V_L of the conventional devices, and the second tail looks like the tail of the conventional devices **[74].** Indeed, it has been reported that the conventional device I_{CP}–V_L presents one current tail for V_L smaller than V_{th}−ΔV_G **[75].** This tail was theoretically calculated and compared with experiments **[74, 75]**. They obviously found a very good correlation between calculated and measured data. However, they did not include the LOCOS edge effect in their calculations to evaluate the slope of the falling side

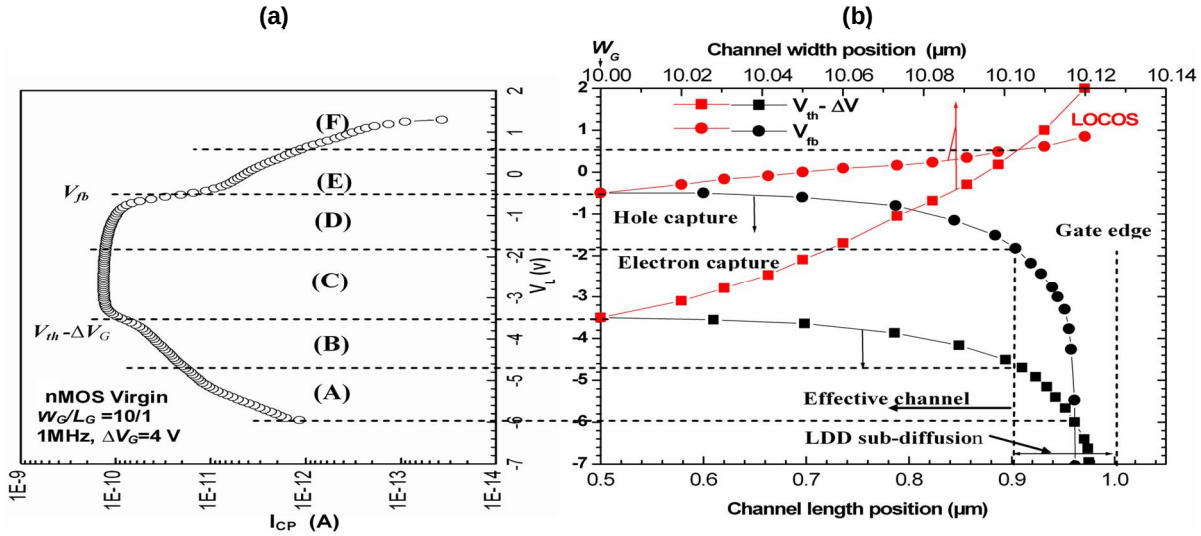

Fig. 11. Constant-amplitude CP measurements in the effective-channel, LDD-subdiffusion, and LOCOS-edge regions. **(a)** I_{CP}–V_L curve of LDD-nMOSFET transistor with W_G/L_G = 10/1 in logarithmic scale. **(b)** Distributions of V_{th} and V_{fb} in the effective-channel, (black lines) LDD-subdiffusion, and (red lines) LOCOS-edge regions. The V_{th} distribution is shifted downward by ΔV_G = 4 V. For specified V_L, the intersection area between V_{th} and V_{fb} curves determines the region of the total capture of both electrons and holes. Scanned regions are **(A)** −6 V < V_L < −4.7 V: the LDD-subdiffusion only. **(B)** −4.7 V < V_L < −3.5 V: the LDD-subdiffusion and effective-channel. **(C)** −3.5 V < V_L < −1.8 V: the LDD-subdiffusion, effective channel, and LOCOS. **(D)** −1.8 V < V_L < −0.5 V: the effective-channel and LOCOS-edge. **(E)** −0.5 V < V_L < 0.6 V: the LOCOS-edge only. **(F)** V_L >0.6 V: leakage current **[38]**. Reproduced with permission from Tahi et *al.*, IEEE Trans. Device Mater. Reliab.10(1), 108-115 (2010). Copyright 2010 IEEE Publishing.

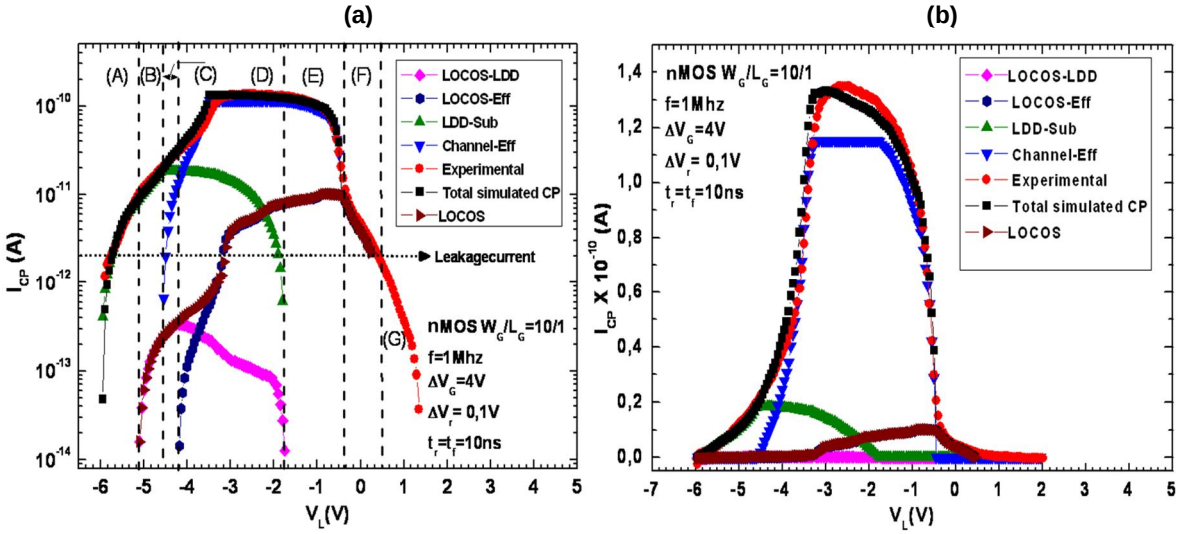

Fig. 12. Comparison between experimental and calculated I_{CP}–V_L characteristics of LDD-nMOSFET with W_G/L_G = 10/1. **(a)** Current in logarithmic scale. **(b)** Current in linear scale. The CP conditions are: V_R = 0.1 V, ΔV_G = 4 V, *f* = 1 MHz, *tr* = *tf* = 10 ns **[73].** Reproduced with permission from Tahi *et al*., IEEE Trans. Electron Devices. 57(11), 2892-2901 (2010). Copyright 2010 IEEE Publishing.

of the I_{CP}–V_L curves. Some authors **[76, 77]** have found a similar I_{CP}–V_L calculation and experiment agreement regarding the I_{CPmax} at the interface and inside the oxide but different I_{CP}–V_L rising and falling edges. In **Fig. 12**, not only the rising edge of the I_{CP}–V_L curve is calculated, but also the falling edge by including the LOCOS effect. This last part of I_{CP}–V_L presents a good correlation with the experimental I_{CP}–V_L characteristics for all transistors. It is influenced by doping nonuniformity and the variation of oxide thickness in the LOCOS region (bird-beak oxide) **[73]**.

3. PERIOD 2005-2015

A. DMN/CDTA-Setup: Generation-4 (2005)

In 2005, DMN acquired a Cascade Microtech Summit semi-automatic probe station for Radio Frequency (RF) and I-V/C-V measurements on wafer level. It is controlled by Nucleus software and allows access to full measurement ranges of parametric test instrumentation with low noise, leakage capacitance, and settling times. This solution permits more experiments and more test data collection for device characterization and wafer-level reliability. In addition, the DMN completed its benches by other Agilent instruments, such as RF Vector Network Analyzer (VNA, Agilent 8753ES), RF Signal Generator Synthesizer (SGS, Agilent 8648D), and Spectrum Analyzer (SA, Agilent E4407B).

a) Low noise amplifier characterization

This new bench carries out radio frequency integrated circuit (RFIC) measurements. In fact, using the setup illustrated in **Fig 13**, the RF measurements were achieved on reconfigurable inductor-less CMOS low noise amplifier (LNA) for multi-standard wireless applications **[78, 79]**. The characterized LNA prototype was fabricated using 0.13 µm CMOS technology. The die area including pads and decoupling capacitors is 0.165 mm^2 **[79]**. However, the active area including decoupling capacitors is 0.052 mm^2 (250 µm × 210 µm). The fabricated LNA includes a source follower as an output buffer to drive the 50 Ω input impedance of the network analyzer.

The measured results for applied gate voltage (V_G) fixed at 0.6 V, at which the power gain reaches its maximum, meaning that the gyrator achieves its high quality factor are given in **fig. 14 [79]**. In **Fig. 14 (a)**, the power gain is tuned from 1.8 to 2.4 GHz by a continuous tuning of the varactor's voltage (Vctrl), where more than 22 dB is performed at 1.8 GHz for Vctrl = 0 V. However, when Vctrl increases, the inductor's quality factor decreases, leading to a lower power gain of 20.6 dB at 2.4 GHz for Vctrl = 1.2 V. Owing to the impact of the first stage on noise contributions, the measured NF is not affected by the Vctrl variations where it slightly varies between 3.2 and 3.5 dB in the frequency range of 1.8–2.4 GHz as shown in **Fig. 14 (b)**. In **Fig. 14 (c)**, the current reuse stage, in charge of input matching, achieves a good S11 lower than −12 dB for all bands of interest. A good output matching is also ensured by a low S22 < −14 dB. As a result, the continuous tuning by Vctrl increases the robustness of the LNA against process variations and allows an easy frequency shift to the target standards. By including the buffer nonlinearities, the IIP3 is also measured across the band, showing moderate values from −16 to −11.8 dBm as given in **Fig. 14 (d).** From a supply voltage of 1.2 V, the LNA power consumption is about 13.8 mW including the buffer and 9.6 mW without it **[79].**

b) Bulk acoustic wave device characterization

Furthermore, the RF VNA was used to characterize electroacoustic resonators elaborated

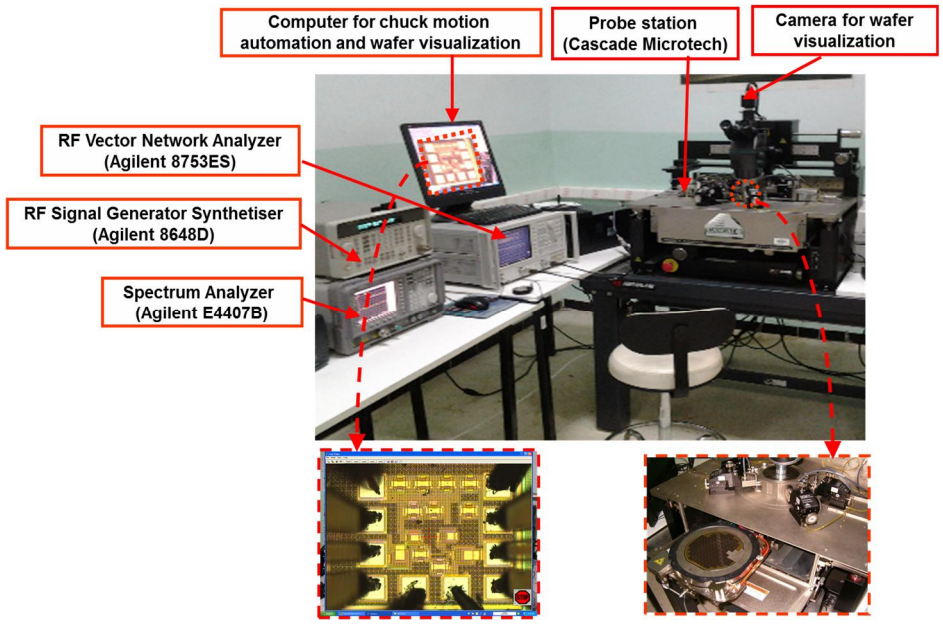

Fig. 13. Experimental Setup_Generation-4 (2005), showing Cascade probe station and RF-Agilent instruments used for RF characterization of semiconductor devices.

by pulsed laser deposition (PLD) of piezoelectric ZnO thin films for bulk acoustic wave (BAW) devices **[80-82]**. The electrical characterization results of ZnO on Al and on Pt samples (deposited at 300 °C, time deposition 3 h) are presented in **Fig. 15**. The results show the S11 return losses obtained by the network analyzer measurements (inharmonic regime) in the range from 0 to 600 MHz, where three resonance frequencies are observed. The fundamental mode appears at 158.2 MHz, the second and the third harmonics at 317 and 476.3 MHz, respectively, for both Al and Pt BAW's bottom electrodes. The fall of the return losses below −10 dB indicates that there is less acoustic energy loss in the piezoelectric material; this is associated with the high crystalline quality of the deposited ZnO on both Al and Pt BAW's bottom electrode. For the Al bottom electrode, the S11 parameter reaches the value of −25 dB for the second mode of resonance (see **Fig. 15**), whereas for Pt bottom electrode, S11 is around −17 dB. Although the ZnO on Al (at 300 °C) presents an amorphous phase part, **Fig. 15** shows that the BAW resonator with Al bottom electrode presents higher performance in the second and third modes compared to that with Pt bottom electrode **[82].**

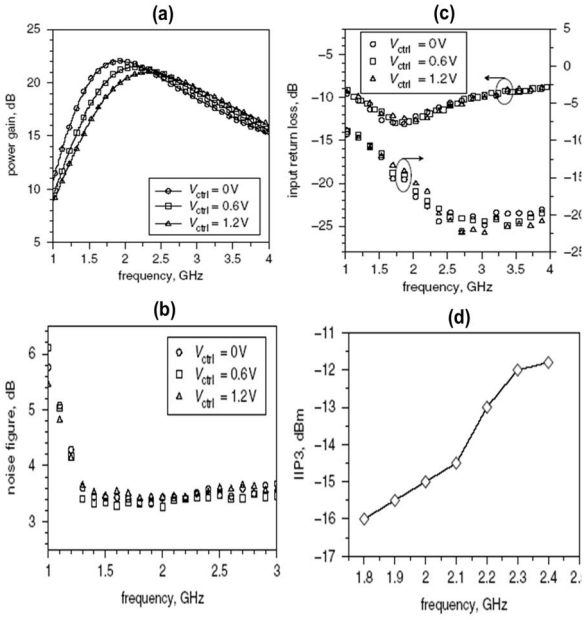

Fig. 14. Measured performances for V_G = 0.6 V and different Vctrl. **(a)** Power gain, **(b)** Noise figure, **(c)** S11 and S22, **(d)** IIP3 **[79]**. Reproduced with permission from Slimane *et al.*, Electrons Letters 50(12), 892-893 (2014). Copyright 2014 IET Publishing.

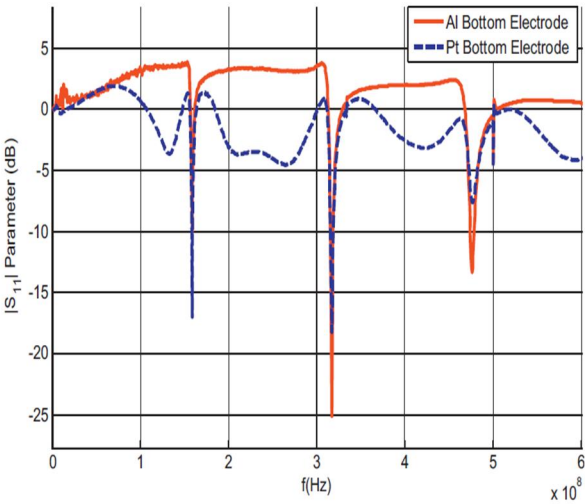

Fig. 15. Measured results of the return loss parameters of the BAW **[82].** Reproduced with permission from Serhane *et al.*, Applied Surface Science, 288, 572-578 (2014). Copyright 2014 Elsevier Publishing.

B. DMN/CDTA-Setup: Generation-5 (2011)

Thanks to heat system designed and fabricated in our division and mounted in Karl-Süss probe station, we have been able to elevate the temperature of the device under test (DUT) and conduct studies on failure modes, such as hot carrier injection (HCI), time dependent dielectric breakdown TDDB), electromigration, and negative bias temperature instability (NBTI). The heat system consists of a hotplate of 30 × 20 mm^2 and a Pt100 sensor to measure temperature. The system delivers temperature up to 200 °C and is powered by a programmable power supply (Tektronix, PS2521G). The heat control is done by a proportional integral derivative (PID) algorithm and is automated using LabVIEW program. The setup including hotplate system for NBTI reliability characterization is illustrated in **Fig. 16**.

To apprehend the NBTI phenomenon root causes, many experimental investigations on MOS devices **[39-44, 83-108]** and circuits **[45, 109-112]** were carried out by our researchers using the setup of **Fig. 16**. Understanding the fundamental physical mechanisms of trap creation and recovery under NBTI conditions is required for developing an accurate predictive model to assist designer for reliability award design and check NBTI impact on analog/digital circuits. To reduce the rapid recovery of NBTI, several on-the-fly electrical characterization methods have been proposed, such as on-the-fly oxide-trap (OTFOT) **[39]**, two-point capacitance-voltage (TPCV) **[41]**, on-the-fly border-trap (OTFBT) **[40],** on-the-fly interface-trap (OTFIT) **[113],** and on-the-fly V_{th} (OTF-V_{th}) **[114].** The concept of TPCV, OTFBT, and OTFOT was developed at DMN and validated on MOS capacitors and transistors fabricated by 1-µm CMOS process of ISiT and 0.18-µm CMOS process of Taiwan Semiconductor Manufacturing Company (TSMC) via Europractice, IMEC. The 0.18-µm test chip was designed at CDTA and fabricated using twin-well technology with shallow trench isolation (STI), lightly doped drain (LDD) surrounded by implanted pocket regions and with a 4 nm thick gate oxide layer grown in dry O_2, and Cox of about 7.35 × 10^{-7} $F.cm^{-2}$. The validation test was performed using the test bench of **Fig. 16**.

a) Electrical extraction methods of NBTI-induced traps

The results of OTFOT method are presented in **Fig.17**. The graphical approach for determining the contribution of stress-induced traps is illustrated in **Fig. 17 (a)**, where M and I denote measure and intermediate values, respectively. The straight lines are the charge recombined by cycle at high and low frequencies, $Q_{CP,H}$ and $Q_{CP,L}$, respectively. From data fits, the intermediate values of the maximum of I_{CP} (or Q_{CP}) can be determined by interpolation for each measurement time. Using alternatively high and low frequencies, OTFOT method separates the NBTI-induced interface-traps (ΔN_{it}) and border-trap (ΔN_{bt}) (switching oxide-trap) densities independently as well as their contributions to the threshold voltage shift (ΔV_{th}), without needing additional method **[39].** The experimental results of ΔN_{it} and ΔN_{bt} densities as a function of stress voltage and temperature in log–log scale are shown in **Fig. 17** (b), the right axis presents the voltage shifts induced by interface and border traps. The NBTI stress-induced ΔN_{it} and ΔN_{bt} time characteristics show an evident power-law time-dependence t^n for both interface-trap and border-trap with an exponent n of 0.16–0.17 and 0.03–0.08, respectively. These results are in perfect

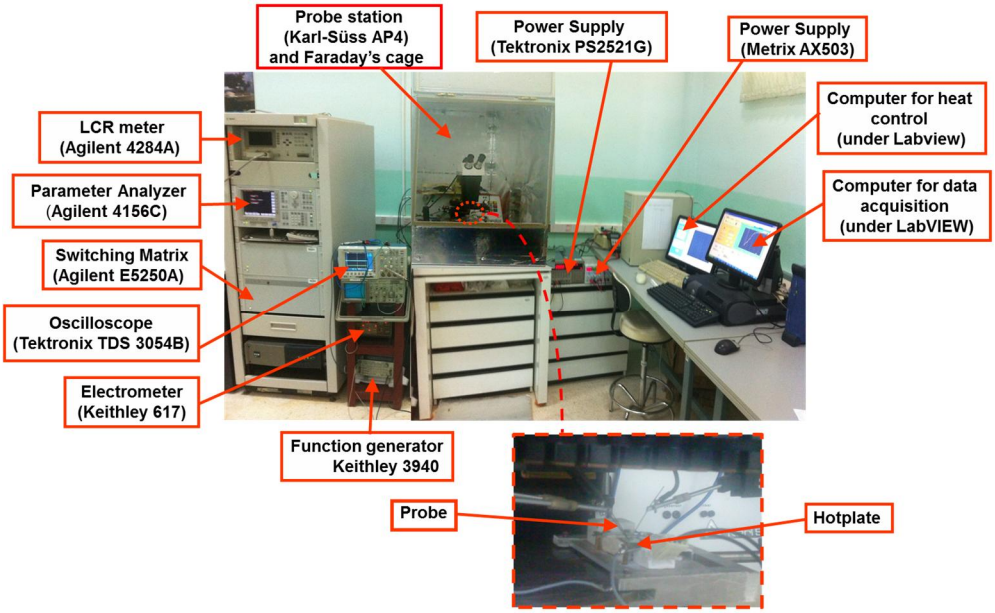

Fig. 16. Experimental Setup_Generation-5 (2011), showing hotplate and instruments used for NBTI experiments on MOS devices and implementing on-the-fly methods.

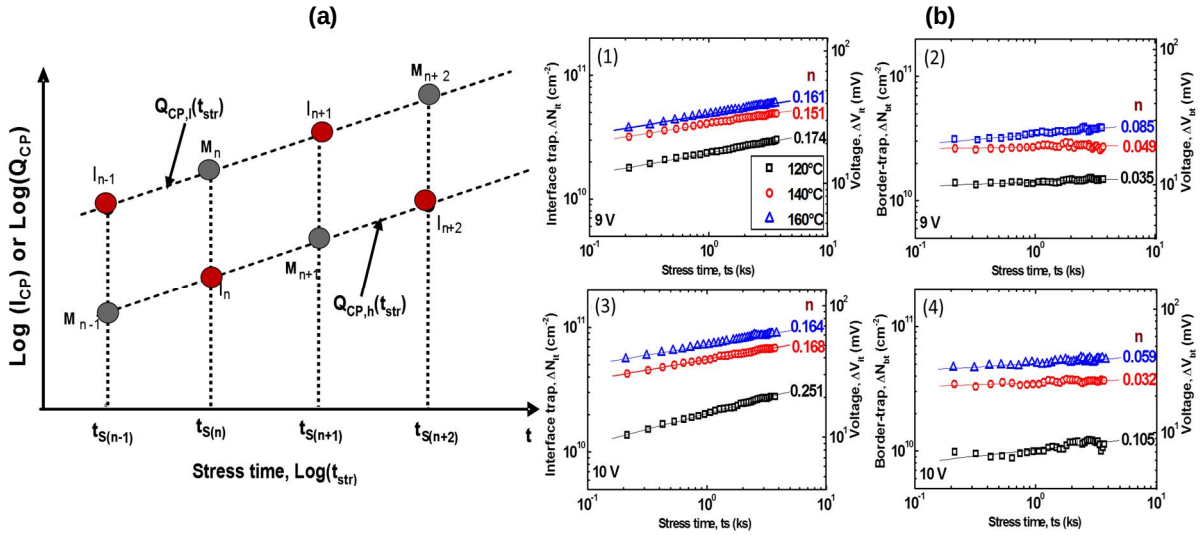

Fig. 17. (a) Illustrative approach for extracting the contributions of NBTI induced interface-trap, ΔN_{it} and border-trap ΔN_{bt}. (b) NBTI stress-induced ΔN_{it} and ΔN_{bt} (on the left axis) as well as their contributions to voltage shift ΔV_{it} and ΔV_{bt} (on the right axis). **(1)** and **(2)** NBTI-induced interface-trap at 9 and 10 V, respectively. **(3)** and **(4)** NBTI-induced border-trap at 9 and 10 V, respectively **[39].** Reproduced with permission from Djezzar *et al.*, Jpn. J. Appl. Phys. 51, 116602 (2012). Copyright 2012 JIP Publishing.

agreement with those previously published by different research groups **[115-117]**.

The bench setup of **Fig.16** has also been used to validate the developed model **[88-96]** of CP geometric component (GC) **[118]** as well as the experimental procedure to extract and eliminate GC current from CP current in NBTI and radiation degradations **[93].** The GC model was extended to polycrystalline silicon thin-film transistors (TFT) **[90].** Contrarily to traditional believe that the geometric component is a parasitic current polluting CP current, we demonstrated that it can be used to estimate the NBTI-induced mobility degradation when using CP-based methods **[94, 96]**. The model fits well data from transistors of 0.18, 1, and 2 µm technologies **[94]. Fig. 18** presents the mobility degradation ($\Delta\mu_p/\mu_{p0}$) as a function of NBTI-induced ΔN_{it}, for stress temperature of 80, 100, and 140 °C with stress bias of $V_S = -2$, 4 V in different pMOS transistors of 0.18 µm technology with fixed gate width and different gate lengths **[94].** The thermal activation energy (E_a) around 0.15 eV is extracted by the Arrhenius plot given inset the figure, E_a is in the range of 0.11 – 0.2 eV, similar to that reported for the interface traps in **[119].** $\Delta\mu_p/\mu_{p0}$ increases with stress time and ΔN_{it}, according to the model (see continues line). This can be also obtained from the mobility degradation model caused by Coulomb scattering, due to the interface trap charge given by **[120].** α_{it} is the parameter describing the effect of interface trapped charge on mobility and is found to be nearly the same for all stress temperatures, as shown on **Fig. 18** This is probably due to the fact that α_{it} is process dependent and here we have investigated devices fabricated by the same process.

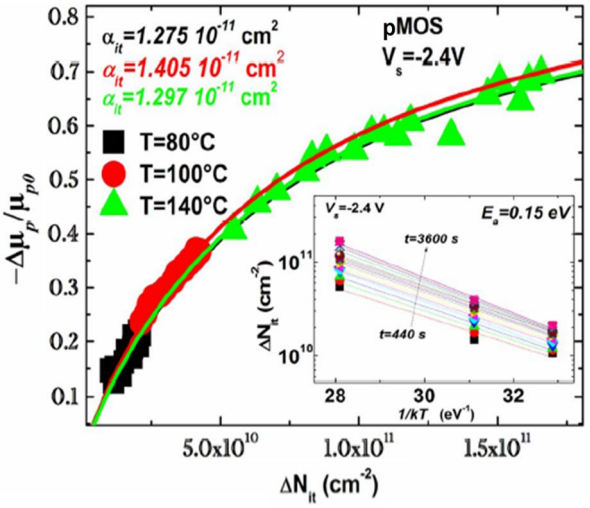

Fig. 18. NBTI-induced mobility degradation extracted by the proposed method as a function of NBTI-induced interface trap (ΔN_{it}). The extraction of activation energy (E_a) is also shown inset the figure **[94].** Reproduced with permission from Tahi *et al.*, IEEE Trans. Device Mater. Reliab. 15(4), 567-575 (2015). Copyright 2015 IEEE Publishing.

b) NBTI permanent component

Moreover, lateral and vertical profiles of NBTI permanent component in pMOSFETs were extracted, using setup of **fig. 16**, along the channel length **[43]** and in depth into the oxide **[44],** respectively. In fact, on one hand, combining simultaneously OTFIT and the reverse voltage variation of source and drain (S/D) during measurement phase of measure/stress/measure (MSM) sequences, we were able to scan NBTI-induced traps across the channel length of pMOS

transistors. The experimental results reveal an evident propagation of the NBTI degradation **[43].** As illustrated in **Fig. 19 (a)**, this propagation seems starting from S/D channel edges and penetrates into the channel center. It is accelerated by temperature and electric field until saturation. However, field-accelerated propagation is more important than temperature-accelerated one **[43].** Further, transistors with shorter channel length degrade more rapidly than those with longer channel length. We have also shown that the channel length has a great effect on NBTI features such as the apparent activation energy and time power-law exponent. These results suggest that diffusion-limited process is not the sole source of the time degradation dependence, but also gate length has to be taken into account. On the second hand, using multi-frequency charge pumping (MFCP) method **[121],** we were able to extract depth profile of NBTI-induced border trap (N_{bt}) in the interfacial oxide region of pMOS **[44]. Figure 19** (b) gives the distribution of the volume trap density ($n_T = dN_T/dZ$), contributing to the permanent component, as a function of the depth, Z. Trap density profile lies between 5 and 7 Å **[44].** The lower the frequency, the thicker the scanned region (for example for f = 1 kHz, Z = 9 Å). In addition, NBTI-induced n_T increases and tends to saturate with stress voltage and looks propagating in the sub-oxide. As schematically illustrated on the top of **Fig. 19 (b)**, the border traps are most likely concentrated in the transition layer, where $O_{3-x}Si_xSi$–H defect family is dominant **[44].** From the above picture, Si–H dipole, which is commonly used to interpret NBTI, is spatially scattered in the interfacial region and differently bonded to various O/Si configurations. Consequently, the basic physical and chemical processes that drive the NBTI phenomenon have different time constants and activation energies. That is why the exponent n is temperature, and field dependent in the time scope of our experiments **[44].**

c) NBTI recoverable component

We also investigated the NBTI recoverable component in MOSFETs using current–voltage (I–V) and charge pumping (CP) techniques. As shown in **Fig. 20**, the experimental results revealed a turn-around phenomenon in threshold voltage shift (ΔV_{th}) of n-type MOS transistors (nMOSFET) during stress phase. The same phenomenon is observed in maximum CP current shift (ΔI_{CPmax}) (not shown here) **[106]. Fig. 20 (a)** plots ΔV_{th}, normalized to its maximum, $\Delta V_{th}/\Delta V_{th\_Max}$ as a function of the stress time for n and pMOSFETs under NBTI stress of V_S = - 12 V (E_{ox} = - 6 MV/cm) at 100 °C **[106].** For pMOSFET, it is clear that ΔV_{thp} exhibits a conventional behavior, i.e. ΔV_{th} shows almost a continuous negative shift (continuous increase in absolute value) during stress phase. However for nMOSFET, ΔV_{thn} does not increase steadily, but rather presents a turn-around phenomenon. At the

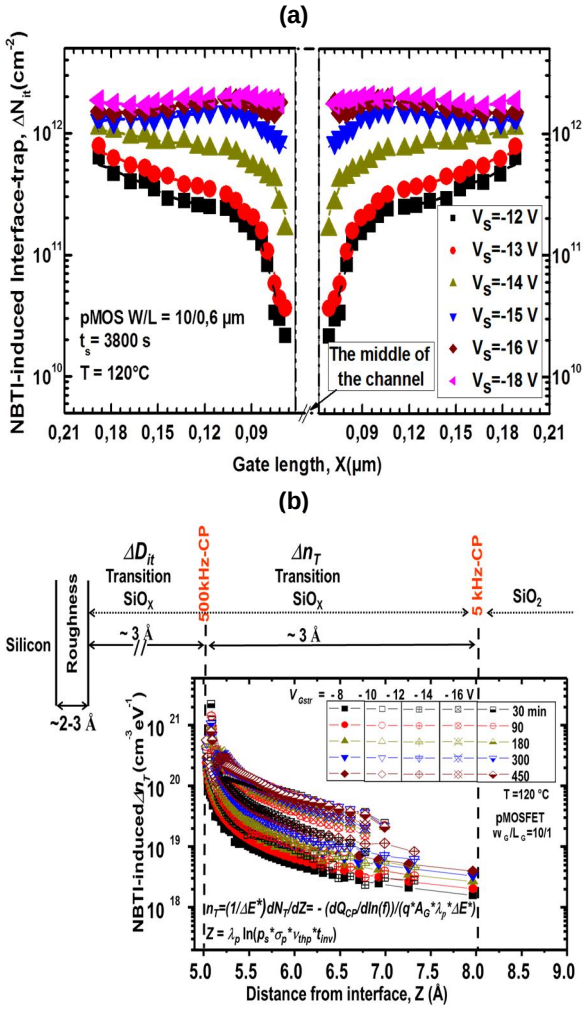

Fig. 19. **(a)** Lateral profiling of NBTI-induced interface-trap, ΔN_{it} in the channel for different stress voltages at stress time of 3800 s and temperature of 120 °C **[43]. (b)** Vertical profiling of NBTI-induced traps in the interfacial oxide region as a function of depth. Onset is qualitative schematic position of the scanned traps **[44].** Assuming that traps, responding at CP-500 kHz, are interface traps and all those below to 5 kHz are considered as border traps. **(a)** Reproduced with permission from Djezzar *et al*., Solid State Electron. 82, 46–53 (2013). Copyright 2013 Elsevier Publishing. **(b)** Reproduced with permission from Djezzar *et al*., Solid State Electron. 106, 54–62 (2015). Copyright 2015 Elsevier Publishing.

beginning of the stress, ΔV_{thn} increases with stress time then it decreases. In fact, at the first stage of the stress time, the creation rate of the interface traps is more important than that of the oxide traps ($dN_{it}/dt > dN_{ot}/dt$) and the interface trap density is greater than that of the oxide trap ($N_{it} > N_{ot}$). Hence, ΔV_{thn} shifts positively. In the second stage of the stress time, ΔV_{thn} decreases but remains positive, because $dN_{it}/dt < dN_{ot}/dt$ and $N_{it} > N_{ot}$. In the last stage of the stress time, both trap density and generation rate of the oxide traps are dominating (i.e. $dN_{it}/dt<dN_{ot}/dt$ and $N_{it} < N_{ot}$) and subsequently

ΔV_{thn} becomes negative. Therefore, at the beginning, ΔV_{thn} is controlled by the permanent component build-up, which could be assigned to the interface trap creation **[106, 107].** This statement does not mean neither all nor only the interface traps are created, but they are the dominant component.

Turn-around phenomenon allows the separation of interface traps (permanent) and interfacial oxide traps "border traps" (recoverable), giving a deeper insight into the dynamic of traps build up under NBTI conditions. The ability of separation comes from the fact that interface and oxide traps induce opposite shifts in ΔV_{th}. Contrarily to NBTI/nMOSFET, NBTI/pMOSFET is unable to achieve trap separation because both trap types induce shifts in the same direction. Exploiting this phenomenon, we have been able to follow the evolution of the degradation over the stress time. **Fig. 20 (b)** presents both NBTI stress and recovery phases: ΔV_{th} shift as a function of stress and recovery times for nMOSFET **[107].** Devices were stressed at V_S = −12.5 V for two hours and recovered at V_R = 2 V for one hour at temperature T_S = T_R = 100 °C. The first phase is extensively explained above in **Fig. 20 (a).** The recovery of ΔV_{th}, illustrated in the right side of **Fig. 20 (b),** is calculated by differentiating ΔV_{th} at end-of-stress (EoS) and ΔV_{thn} at end-of-recovery (EoR) **[107].** It is clear that ΔV_{th} shifts positively, when V_{GS} is swept from stress voltage (V_S = − 12.5 V) to recovery voltage (V_R = 2 V), suggesting that the reversible part is dominated by the positive charges, while the negative charges, that were shaded during stress, become visible during recovery phase. To get more insight on ΔV_{th} behavior during recovery phase, we conducted NBTI stress/relaxation cycle measurements on nMOSFET. The recovery phase has shown the contribution of three components to V_{th} shift (ΔV_{th}) in nMOSFET, as illustrated in **Fig 20 (c)**. One component is permanent (ΔV_{thP}) and dominated by interface traps, created during stress at the Si/SiO_2 interface. The other components are oxide traps, generated in the interfacial oxide region. Both traps are positively charged; one is cyclic (ΔV_{thC}), while the other is totally recoverable (ΔV_{thR}) **[107].**

d) NBTI in MOS capacitor

As shown above, the influence of gate edges does not allow tracking NBTI degradation in the effective gate length to get a clear picture on the basic mechanisms behind it, especially in short gate lengths **[43, 93, 98].** To overcome this issue and further understand the origin of the NBTI degradation in the main gate channel without edge influence, NBTI experiments were conducted on p-substrate MOS (nMOS capacitor) under accumulation condition using setup of **Fig. 16 [101, 108].** In **Fig. 21**, the expected correlation between the evolution of ΔV_{th} and the evolution of time exponent (n) and activation energy (E_a)

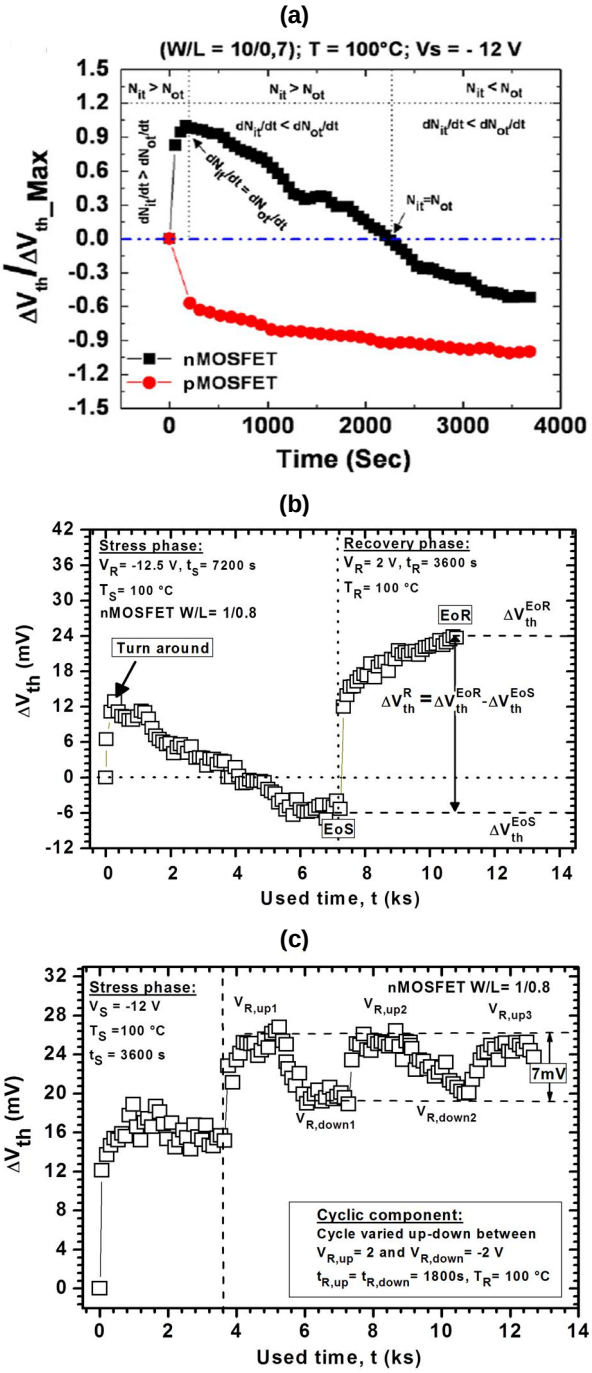

Fig. 20. (a) Time evolution of ΔV_{th}, normalized to ΔV_{th_Max}, ($\Delta V_{th}/\Delta V_{th\_Max}$) for nMOSFET and pMOSFET at Vs = - 12 V and T = 100 °C, the stress is stopped at 200 sec **[106]. (b)** ΔV_{th} as a function of stress time and recovery time of nMOSFET stressed for 2 hours at V_S = − 12.5 V and recovered for 1 hour at V_R = 2 V, and at temperature T_S = T_R = 100 °C **[107]. (c)** NBTI-induced cyclic component of ΔV_{th} as a function of number of cycles at stress voltage V_S = − 12 V for $V_{R,up}$ = 2 V and $V_{R,down}$ = 0 V **[107]. (a)** Reproduced with permission from Benabdelmoumene *et al.*, Solid State Electron. 121, 34–40 (2016). Copyright 2016 Elsevier Publishing. **(b)** and **(c)** Reproduced with permission from Djezzar *et al.*, Microelectron. Reliab. 110, 113703 (2020). Copyright 2020 Elsevier Publishing.

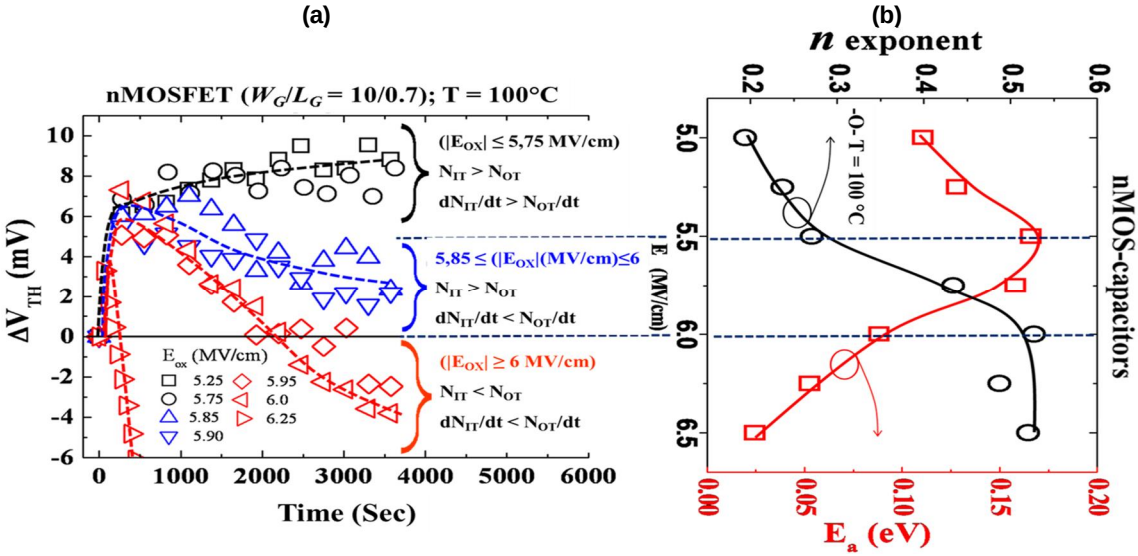

Fig. 21. Correlation between temporal evolution of nMOSFET ΔV_{th} **(a)** with Ea and *n* exponent electrical field dependence of nMOS-capacitor **(b) [108].** Reproduced with permission from Benabdelmoumene *et al*., IEEE Trans. Device Mater. Reliab. 18(4), 583-591 (2018). Copyright 2018 IEEE Publishing.

parameters, extracted from flat band shift, ΔV_{fb} **[108]. Fig. 21 (a)** presents the temporal evolution of ΔV_{th} for different electric fields, E_{ox}. Here, we should note that E_{ox} is refined to be able to track the different phases; before, during, and after the turnaround phenomenon because the latter is very sensitive to electric field. In the other words, the dominance of oxide traps occurs promptly under E_{ox} and it is more important on a large range of E_{ox}, and thus it shadows (compensates electrically) the interface traps quickly. **Fig. 21 (b)** gives the variation of E_a and n as a function of E_{ox}. Obviously, the phases previously observed in n and E_a are almost corresponding to those observed in ΔV_{th} of nMOSFET. The dashed lines between **Figs. 21 (a)** and (b) are only drawn as guide to eye. E_a and n parameters go through three distinct phases with respect to the electric field stress **[108].**The two first phases are found to be governed by either interface or oxide traps depending on the amount and the rate generation of each one. The second phase is fast and presents a transition phase between NBTI and SILC phenomena. This latter dominates the third phase of the degradation. These findings have been confirmed by the appearance of the turn-around effect in nMOS transistors under NBTI stress [see **Fig. 21 (a)**] **[106].** Moreover, CP characterization has unveiled that NBTI degradation in nMOS transistor goes through two stages [106]. First, only interface traps are created, and then simultaneous generation of interface and oxide traps takes part.

e) NBTI in integrated circuits (ICs)

On the other hand, experimental investigations on the impact of NBTI stress at circuit-level were carried out **[45,109-112].** Measure/stress/measure protocol was applied on CMOS inverter to analyze the impact of dynamic NBTI stress on inverter dc

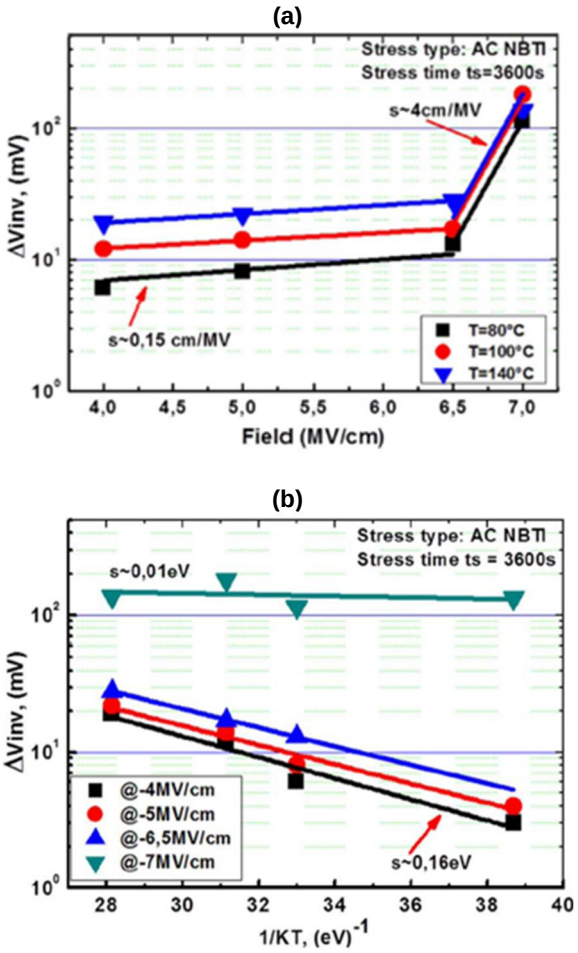

Fig. 22. Inverter logic threshold shift due to ac NBTI with respect to the applied field in (a) and to the temperature in (b**) [45].** Reproduced with permission from Chenouf *et al*., IEEE Trans. Device Mater. Reliab. 16(3), 290-297 (2016). Copyright 2016 IEEE Publishing.

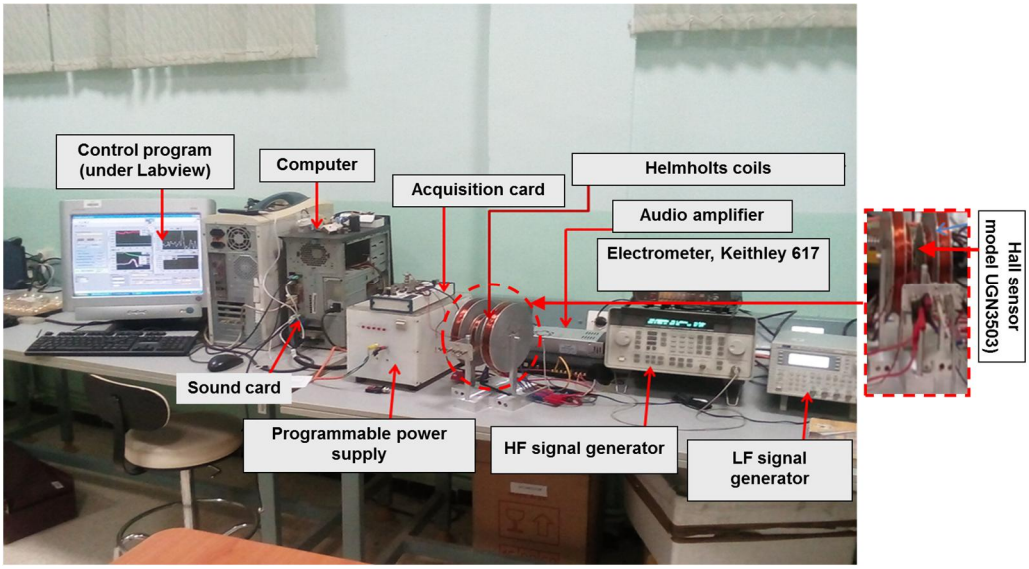

Fig. 23. Experimental Setup_Generation-6 (2015), illustrating Helmholtz coils and instruments used for EDMR experiments.

response and temporal performance and attempt to correlate circuit-level NBTI degradation with that of device-level (pMOSFET) **[110-112, 122, 123]. Fig. 22** shows the AC NBTI-induced shift of inverter logic threshold (ΔV_{inv}), plotted in a semi-log scale, as a function of the oxide field in (a) and the temperature in (b) **[45].** In **Fig. 22 (a)**, under AC NBTI stress with oxide field up to 6.5 MV/cm, the electric field acceleration parameter (γ) of ΔV_{inv} is almost constant and equals 0.15 cm/MV. Then, it rises to 4 cm/MV when the electric field goes higher. The results show that ΔV_{inv} increases with increasing electric field and worsens at elevated temperature. The opposite trend can be observed for the activation energy value (see **Fig. 22**). This latter equals 0.16 eV under AC NBTI with low oxide field, then it drops to 0.01 eV under higher oxide field. Consequently, ΔV_{inv} shows two tendencies: degradation with low field acceleration (0.15 cm/MV) and high activation energy (0.16 eV) then degradation with high field acceleration (4 cm/MV) and low activation energy (0.01 eV). These two different temperature dependencies of ΔV_{inv} seem to point toward the co-existence of two physical mechanisms behind the NBTI degradation of the pMOS threshold shift (ΔV_{thp}) to know: interface traps creation (with 0.16 eV) and holes trapping (0.01 eV) **[115, 123]**. The analysis of such behaviour when correlated with the pMOS threshold shift points toward the coexistence of more than one physical mechanism behind the degradation, where one mechanism could dominate the other under certain stress conditions. Depending on these conditions, circuit lifetime could be more or less affected **[45, 110-112].**

4. PERIOD 2015-2025

A. DMN/CDTA-Setup: Generation-6 (2015)

a) Magnetic field effect on NBTI stress

Introduction of Helmholtz coils (made in-house) in our domestic experimental setup allowed combining electrical characterization with magnetic field. Using magnetic field, new investigations on microscopic structures of defects behind the reliability issues and instabilities in MOS devices became possible. The instrumentations of home-made EDMR spectrometer are presented in **Fig. 23**. EDMR technique has proven, through its variants; such as spin dependent recombination (SDR) **[125, 126],** spin dependent trap-assisted tunneling (SDT) **[127]** and spin dependent charge pumping (SDCP) **[128],** to be a powerful tool for investigating the microstructures (atomic scale) nature of defects in semiconductor and electronic devices.

The low magnetic field EDMR setup is mainly based on a set of Helmholtz coils, providing a very uniform magnetic field around the halfway point between the coils. The magnetic field is sensed and controlled using Hall sensor (model UGN3503). The signal is amplified and digitized by main of microcontroller 16F877. The larger coils (outer coils) provide the repeated sweeping magnetic field with maximum field of 200 G and the smaller set (inner coils) provides what is called the modulation magnetic field with maximum field of 20 G. The modulation is used to encode EDMR signal, then after, a virtual lock-in amplifier (VLIA) is used to demodulate the encoded EDMR signal. Thus, experimental noise is attenuated and the signal-to-noise ratio (SNR) is well enhanced. The modulation signal is generated using the output of PC sound

card and amplified by a power audio-amplifier (Sony XM-N502), the modulation frequencies can be in the range of (20 Hz-20 Khz). The spectrometer control program was implemented using LabVIEW software. The program includes the VLIA, PID controller, averaging and Fast Fourier Transform (FFT) programs. At DMN, experimentation on the influence of the magnetic field during NBTI stress and recovery in MOSFET power devices were carried out using CP, I-V, and DC-IV techniques **[129-131].** The investigated devices are commercial p-channel VDMOSFETs IRF 9530 N encapsulated in TO-220 plastic cases, with gate oxide thickness of 100 nm, nominal drain current of 14 A, and drain to source breakdown voltage of 100 V. The NBTI stress/recovery experiments were performed using Agilent HP 4156C for current measurement and Agilent 16440A SMU/pulse generator selector to switch between stress and measure. The devices were stressed up to 900 s by applying - 60 V on the gate at 80 °C, followed by the recovery at zero voltage. Two measurement methods were used; in the first one, the drain current I_{DS} is monitored around V_{th} (at $V_G = -3$ V) with applied drain-source voltage (V_{DS}) of - 50 mV, while, in the second one the maximum charge pumping current (I_{CPmax}) is measured at the drain contact, with the source grounded. The CP measurements are performed using triangular wave with amplitude of 4 V and frequency of 400 kHz. **Figure 24** reports the impact of low magnetic field (B < 10 mT) applied on commercial power vertical double diffused MOS transistor (VDMOSFET) submitted to NBTI stress and recovery **[129].** Threshold voltage shift (ΔV_{th}) and charge pumping current shift (ΔI_{CP}) are given by **Fig. 24 (a)** and **(b)**, respectively. It compares the dynamic of stress and recovery of ΔV_{th} (ΔI_{CP}) with and without applied perpendicular and parallel magnetic field to the Si/SiO_2 interface. All ΔV_{th} (ΔI_{CP}) curves with applied perpendicular (⊥) and parallel (//) magnetic field are the same. Thus, the direction of applied magnetic field does not affect the impact of the magnetic field on NBTI degradation. In the stress phases, both ΔV_{th} and ΔI_{CP} as a function of time curves follow an exponential law **[132, 133]** and are reduced by applied magnetic field. In addition, the characteristic time constant (τ) of ΔV_{th} increases by applied magnetic field, indicating the change of stress dynamic (stress degradation rate) with applied magnetic field, while τ of ΔI_{CP} remains unchanged. The higher magnetic field is the slower stress degradation rate is **[129].**

The recovery phase of ΔV_{th} and ΔI_{CP} are illustrated inset Fig. 24 (a) and (b), respectively. ΔV_{th} recovery curve is normalized to its maximum value in the stress phase (the last stress value) and ΔI_{CP} recovery curves to its minimum value in the recovery phase (the first recovery). It is clear that the applied magnetic field accelerate the recovery of ΔV_{th} [129]. Therefore, regarding the above observation the dynamic of ΔV_{th} is reduced in the

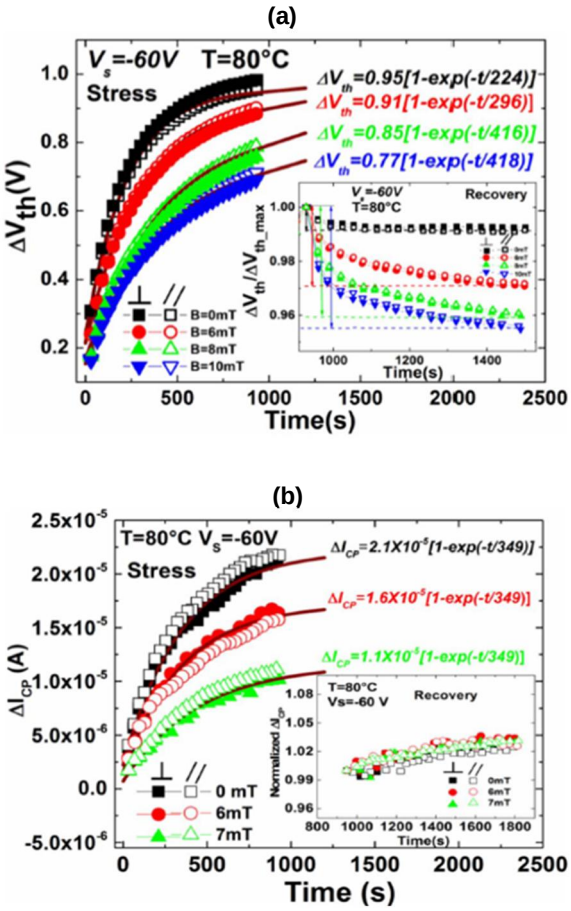

Fig. 24. Comparison between dynamics of stress and recovery with and without applied perpendicular (⊥) and parallel (//) magnetic field to the Si/SiO_2 interface (a) ΔV_{th}, the recovery phase curves are normalized to the last stress values, see inset the figure, (b) ΔI_{CP}, the recovery phase curves are normalized to its first value, see inset the figure **[129]**. Reproduced with permission from Tahi et *al.*, IEEE Trans. Device Mater. Reliab. 17(1), 99-105 (2017). Copyright 2017 IEEE Publishing.

stress phase and pronounced in the recovery phase as the magnetic field goes high. However dynamic of ΔI_{CP} (related to ΔN_{it} shift) is not affected by applied magnetic field during the stress phase and all normalized ΔI_{CP} recovery curves remain the same with and without applied magnetic field [130]. According to above observation, we could conclude that the dynamic of interface trap creation is not affected by applied magnetic field in both stress and recovery phases. However, the magnetic field reduces the dynamic of oxide traps generation and accelerates their recovery **[129].**

b) AC Magnetic field modulation for MOS capacitance-voltage C-V

Using the abovementioned magnetic setup, a new capacitance–voltage technique C-V concept based on surface potential modulation by external ac magnetic field (instead of ac electric field) has been validated **[47, 134].** The validation of the magnetic-mode configuration C-V technique was

performed with fully automated bench using in-house developed Helmholtz coils (described in Section IV.A.1 **[129]**) to generate a sinusoidal magnetic small-signal (ac) superposed to a dc-voltage (offset sweep). The coils are powered by sinusoidal signal, which is generated using TTi-TGA1244 wave-form generator and amplified by main of Sony XM-N502 audio amplifier. The magnetic field is measured by a Hall sensor UGN3503 connected to NI–PCI-6220 acquisition card. The DUT current is amplified using a picoelectrometer Keithley 485 with a resolution of 0.1 pA. The amplified signal is collected at the analog output of Keithley 485 and connected to the input of performed PC sound card (maximum sampling frequency of FS = 44.1 kHz and 24-bit precision). So, the frequencies range of our measurement is only up to 20 kHz. To demodulate the DUT current, a virtual lock-in amplifier (VLIA) is implemented using LabVIEW Software. Data show that the surface potential is modulated using external ac magnetic field **[47].**

The technique is validated on commercial p- and n-type VDMOSFETs with reference IRF9530 and IRF510, respectively. These devices are encapsulated in TO-220 plastic cases and built-in standard silicon-gate technology with 100-nm-thick gate oxide. The needed lateral dimension parameters are extracted using the method described in reference **[135]** for IRF9530 and using those given in reference **[136]** for IRF510. The measured gate–source (C_{GS}) and gate–drain (C_{GD}) capacitances as a function of gate voltage (V_G) for p- and n-type transistors are given in **Fig. 25 [134]**. The surface potential is modulated using a small ac magnetic field of frequency (f) and amplitude ΔB equal to 1 kHz and 4 mT, respectively. **Figure 25** illustrates a comparison between $C_{GD}(V_G)$ and $C_{GS}(V_G)$ characteristics obtained by magnetic and conventional mode configurations. The magnetic mode configuration technique scans different regions of the VDMOSFET, such as P^+-region (source-region), N-region (channel-region), and P-region (drain-region) in different regimes; depletion, accumulation, and inversion regimes. In succinct, the capacitance measured by magnetic mode configuration is different from that obtained by conventional mode configuration in depletion and weak-inversion regimes. However, they are the same for inversion and accumulation regimes, more details and analysis are given in reference **[47].** In addition, combining $C_{GD}(V_G)$ and $C_{GS}(V_G)$ allows extraction semiconductor capacitance (C_{SC}), interface trap capacitance (C_{it}), doping profile concentration N(x), and interface trap density $D_{it}(E)$ of different regions of VDMOSFET **[134].** It is clear that the magnetic mode configuration C-V technique offers a powerful tool to characterize different regions of VDMOSFET for both n- and p-type transistor and extract their technological and electrical parameters.

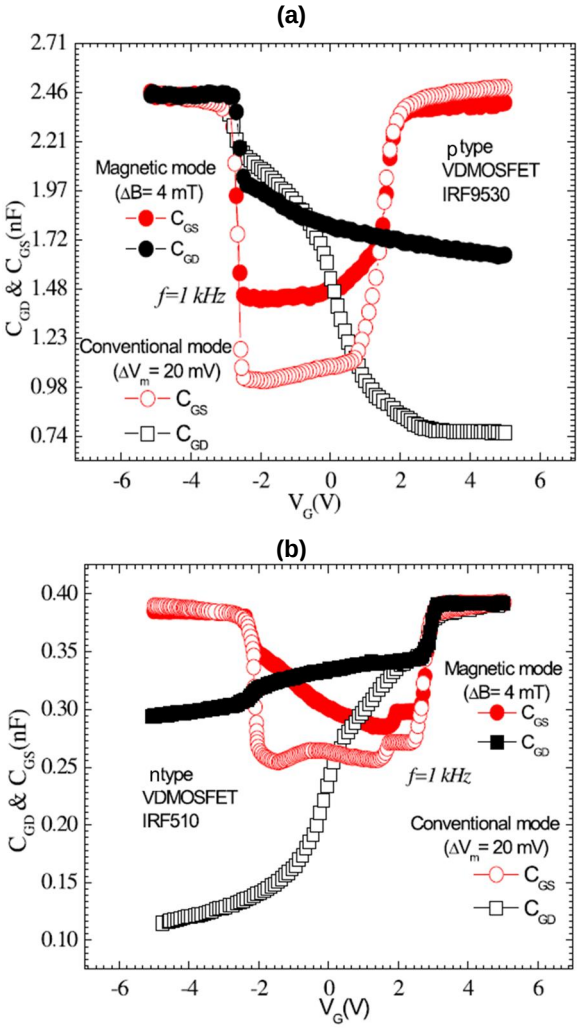

Fig. 25. Comparison between $C_{GD}(V_G)$ and $C_{GS}(V_G)$ characteristics obtained by conventional and magnetic modes configurations. **(a)** For p-type VDMOSFET (IRF9530). **(b)** For n-type VDMOSFET (IRF510) **[47]**. Reproduced with permission from Tahi *et al.*, IEEE Trans. Electron Devices. 68(5), 2173-2180 (2021). Copyright 2021 IEEE Publishing.

B. DMN/CDTA-Setup: Generation-7 (2018)

The As MOSFET electrical characteristics degradation under NBTI stress recovers rapidly after the stress removal, it becomes very difficult to get a complete picture of NBTI-induced traps inside the SiO_2 oxide and/or the stacked gate dielectric using one type of characterization technique, especially a DC technique. This recovery produces strong transients of threshold voltage V_{th} in the wide time range of microseconds to tens of seconds **[137, 138]**. The typical time range of the semiconductor parameter analyzers (Agilent 4156C) is from milliseconds to tens of seconds, which overlaps with that of the transient in device parameters. Consequently, the overlap in time scale must be surmounted by fast measurement

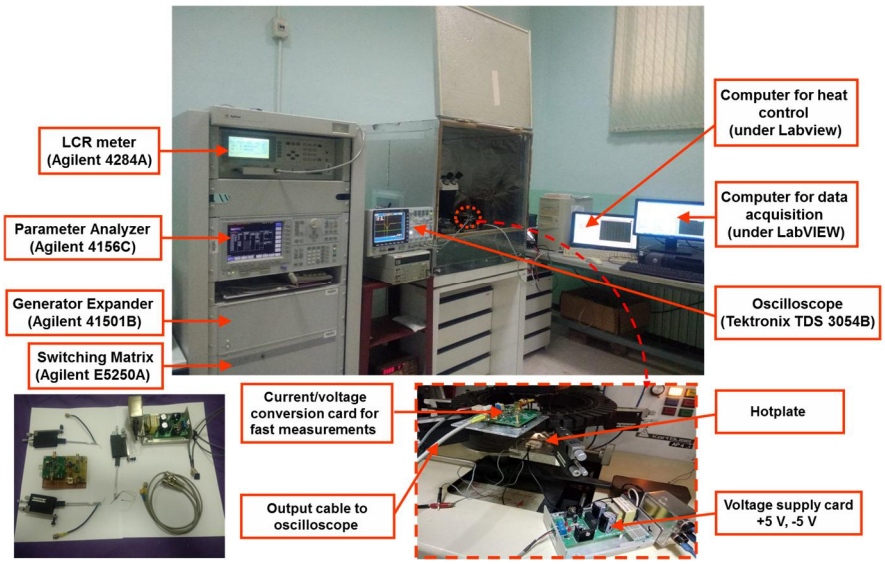

Fig. 26. Experimental Setup _Generation-7 (2018), showing conversion electronic card and instruments used for fast measurements.

techniques to capture the entire fast transient trapping and detrapping phenomena **[48, 137-142].**

a. Electronic card mounted outside the probe handle

Figure 26 presents the fast measurement setup developed in the laboratory of the DMN. It consists in fast pulsed I_{DS}-V_{GS} technique **[139-142].** The MOSFET (DUT) is connected to the operational amplifier (OPA657) configured in trans-impedance mode. The drain current, I_{DS} is basically sensed by the input of OPA657, and then converted into output voltage, V_{OUT} via feedback resistance, R to be displayed/recorded on/in the scope. The recorded voltage is converted back into I_{DS} and analyzed. By virtual short circuit property of OPAMP, the voltages at the two input terminals are approximately equal when negative feedback is present through R. The drain voltage of the MOSFET is thus fixed at V_{DS} supplied by the voltage source. Since the input impedance at the input terminal of OPAMP is very high, the drain current flows entirely through the gain resistor R. In other words, the drain current is measured by the gain resistor R. The electronic card is mounted outside of probe handle, as illustrated in **Fig. 26**.

The fast pulsed I_{DS}-V_{GS} technique was used to characterize NBTI stress in pMOSFET **[139].** Fast-MSM (FMSM) protocol was applied on pMOSFET of 1 µm CMOS technology (fabricated at ISiT) with gate width and gate length of 1 and 0.8 µm, respectively. SiO_2 gate oxide thickness is 20 nm. A high-speed operational amplifier (TI OPA657) was used to measure the transient current, which can achieve fast measurement without requiring expensive instruments. To minimize the parasitic effects, an impedance matching (50 Ohm) was applied and cables were made as short as possible. Signals were carried to the scope using cables of the same length to ensure the synchronization of

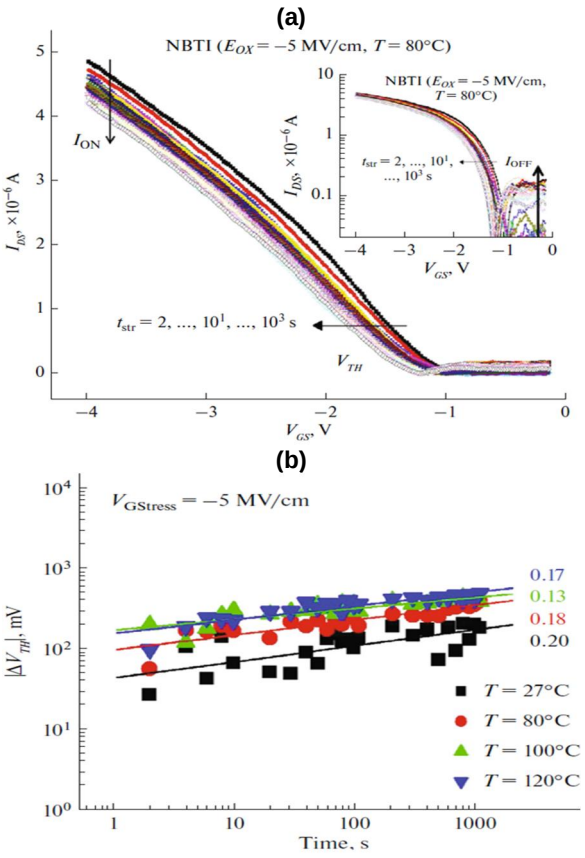

Fig. 27. (a) Fast I_{DS}–V_{GS} transfer characteristic curves as a function of stress time, inset shows semi-log plot of fast I_{DS}–V_{GS} transfer characteristic curves. **(b)** Time evolution of threshold voltage shift, $|\Delta V_{th}|$ and extracted time exponent for pMOSFET for different stress temperatures **[139].** Reproduced with permission from Benabdelmoumene et *al.*, Russian Microelectronics. 52(5), 429-438 (2023). Copyright 2023 Springer Publishing.

V_{GS} and $V_{GS}(I_{DS})$ **[143].** The drain current was measured by the sense resistor R = 10 kOhm. **Figure 27 (a)** shows the evolution of the smoothed fast I_{DS}-V_{GS} curves. They were measured with drain voltage of – 50 mV, during NBTI stress under E_{ox} = – 5 MV/cm and T = 80 °C. I_{DS}-V_{GS} curve obviously shifts toward negative direction and the degradation of I_{ON}/I_{OFF} (I_{OFF} is shown inset **Fig. 27 (a)**) with increasing stress time is due to traps creation in the gate oxide and at the Si/SiO_2 interface. **Figure 27 (b)** gives the time evolution of ΔV_{th} shifts of stressed pMOSFET in Log-Log scales for different stress temperatures (T). ΔV_{th} exhibits the well-known power law time dependence for different NBTI stress conditions, i.e. ΔV_{th} is proportional to t^n. The result is consistent with that found in previous works **[144, 145]**. n is extracted by fitting the experimental data. It is almost the same for different temperatures and is around 0.18. In contrast, we are experiencing a dependence of n with E_{ox}. n increases with increasing E_{ox} in thick oxides (20 nm), suggesting the presence of several degradation mechanisms in the oxide **[138].** However, thin oxides (4 and 2.3 nm) show roughly a constant n of 0.16, indicating the dominance of the interface trap creation from electrical viewpoint **[142, 146]**. Actually, the most oxide traps created during NBTI stress in thin gate oxide are more dischargeable towards the poly-Si and substrate by tunneling process than in thick gate oxide **[147, 148]**. The trapped charges reduce with the oxide thickness. It seems that traps in thick oxides have a great retention ability of charges compared to thin oxides. Therefore, the detrapping process reduces the amount of electrically active defects. Thin oxide even is more defective, it is often better oxide, because it allows detrapping charges. However, thin oxides present high gate leakage current due to stress induced leakage current (SILC) **[149-151].**

b. Electronic card mounted on the probe handle

In this setup, the electronic card of conversion current/voltage for fast measurement is mounted on the probe handle as close as possible to the probe's needle, as shown in **Fig. 28**. We should mention that measurements were carried out using the shortest cabling possible to minimize parasitic and the input/output time delay. The trans-impedance amplifier (TIA) circuit uses a low-noise high-speed OpAmp OPA818. It has a gain bandwidth product (GBP) of 2.7 GHz, low input capacitance of C_{in} = 2.4 pF, and 2.2 nV/√Hz of noise which makes it an extremely versatile. Also, it has a gate field-effect transistor (JFET) input stage for high gains (> 2 kΩ) and a wide supply range from 6 V to 13 V for high-speed and wide dynamic range applications. The OPA818 achieves a fast slew rate (1400 V/µs), which provides high large-signal bandwidth and low distortion. For packaging, the OPA818 is available in an 8-lead WSON package with an exposed thermal pad for heat dissipation. This device is specified to operate over the industrial temperature range of - 40 °C to + 85 °C.

Figure 28 illustrates the experimental bench used to implement the separated single pulse charge pumping (SSPCP) **[48],** developed by semiconductor component reliability team of DMN. It aims to improve the analysis of MOSFET degradation by localizing the interface traps in the transistor channel. The technique is particularly useful for stress-induced trap profiling, allowing deep investigation of nonuniform degradation induced by HCI and NBTI in transistors with short channels. Its setup consists of applying gate pulses, generated using the multifunction synthesizer Keithley 3940. Unlike the conventional single pulse charge pumping (CSPCP) **[152],** where source and drain terminals are connected and I_{DS} is measured, the SSPCP setup separates

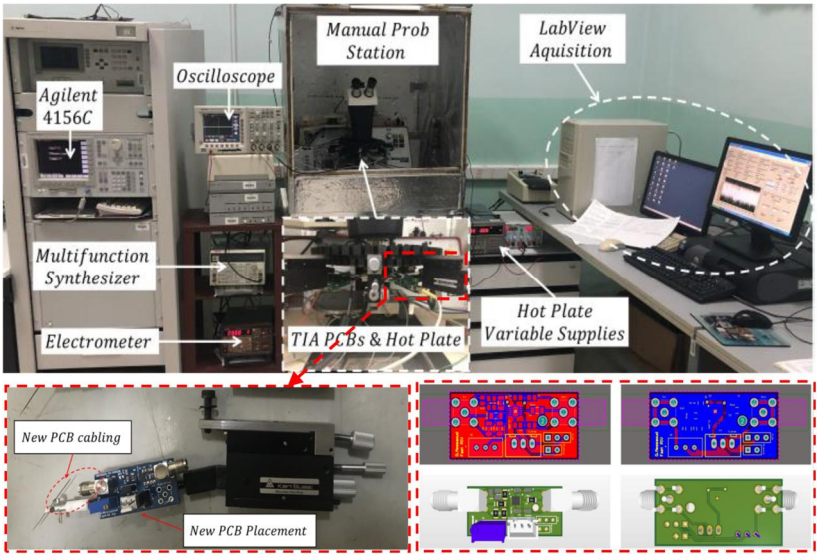

Fig. 28. Experimental Setup_Generation-7 bis (2020), showing conversion electronic card mounted on the probe handle and instruments used for fast measurements.

the source and drain terminals. Therefore, three currents I_D, I_B, and I_S are separately converted into voltages (V_D, V_B, and V_S) using three trans-impedance amplifiers (TIAs). The cards are designed using the low-noise high-speed OpAmp OPA818. The gain (resistor feedback) is set to be 10kΩ for large bandwidth (WB > 60 MHz) input signals, thus faster gate pulses (e.g. 100 ns) **[48].** Furthermore, all the signals including gate pulses (V_G) are visualized using a four-channel oscilloscope (TDS3054B) and saved using the LabVIEW acquisition program. The OpAmps output V_D, V_B, and V_S voltages are reconverted later into currents.

An example of I_D, I_S, and I_B signals, resulted from SSPCP technique applied on MOSFETs of different gate sizes before and after HCI stress for 1 hour, are given in **Fig. 29 [48].** Results show that signals after stress are not identical to those measured before. The degradation can clearly show up in the peaks that appeared inside the dashed circles in the figure. These peaks are presented in the three currents I_D, I_S, and I_B but they are not quantitatively the same. As discussed elsewhere **[152, 153],** interface traps density can be extracted from each current. HCI-induced traps in the drain region are more significant than in the source region **[48].** Therefore, SSPCP offers the advantage of separating the channel into two regions, providing a clear insightful understanding of the phenomena occurring in the source and drain regions, especially when subjected to BTI conditions. This makes it a valuable tool in semiconductor device characterization.

5. SYNTHESIS AND PERSPECTIVES

In addition to physical modelling and simulation scientific research activities **[154-159],** the electrical characterization of semiconductor devices and reliability researches have been conducted at DMN since mid-nineties, where several experimental benches have been built up from simple benches to more complicated ones, as summarized in **Fig. 30**. In-house developments of electrical test bench platforms are mainly motivated by the needs of CDTA clean-room facility to evaluate the reliability of its products, i.e. process yield evaluation and device/circuit lifetime estimation. The evolution curve of **Fig. 30** roughly shows three decades of progress. Each decade is marked by two to three setup generations. In the first decade (1995-2005), the setups were intended for the electrical characterization and extraction of device's characteristics. Moreover, investigations were conducted on reliability issues caused by the ionizing radiation damage in silicon dioxide, SiO_2 and Si/SiO_2 interface of MOSFETs transistors **[50]** as well as development of a reliable test procedure and electrical test n **[160].**

The second decade (2005-2015) was distinguished by the acquisition of Agilent instruments and Cascade Microtech probe station. This equipment opened the road to setup benches

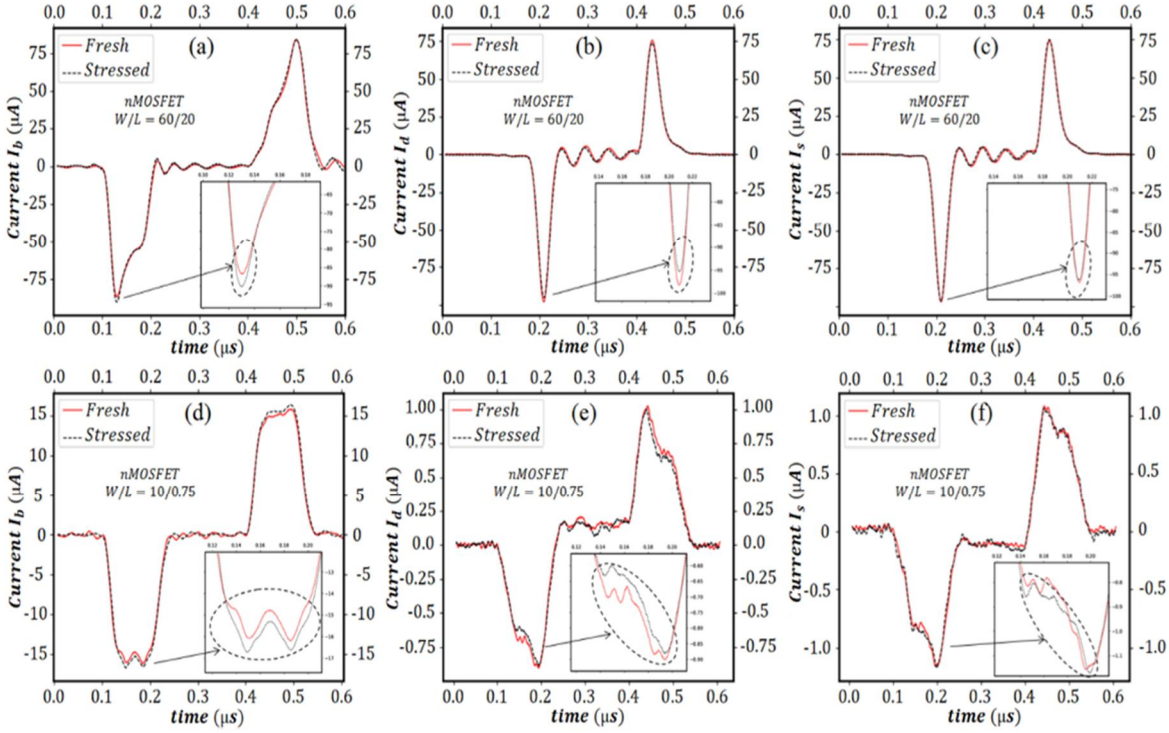

Fig. 29. Fresh measures (continuous line) and after HCI stress measures (dashed line) with $V_G = V_D$ at room temperature for 1 hour on nMOSFET 60/20 and nMOSFET 10/0.75 with **(a)** and **(d)** for substrate current, **(b)** and **(e)** for drain current, and **(c)** and **(f)** for source current **[48]**. Reproduced with permission from Messaoud et *al.*, IEEE Trans. Device Mater. Reliab. 23(4), 521-529 (2023). Copyright 2023 IEEE Publishing.

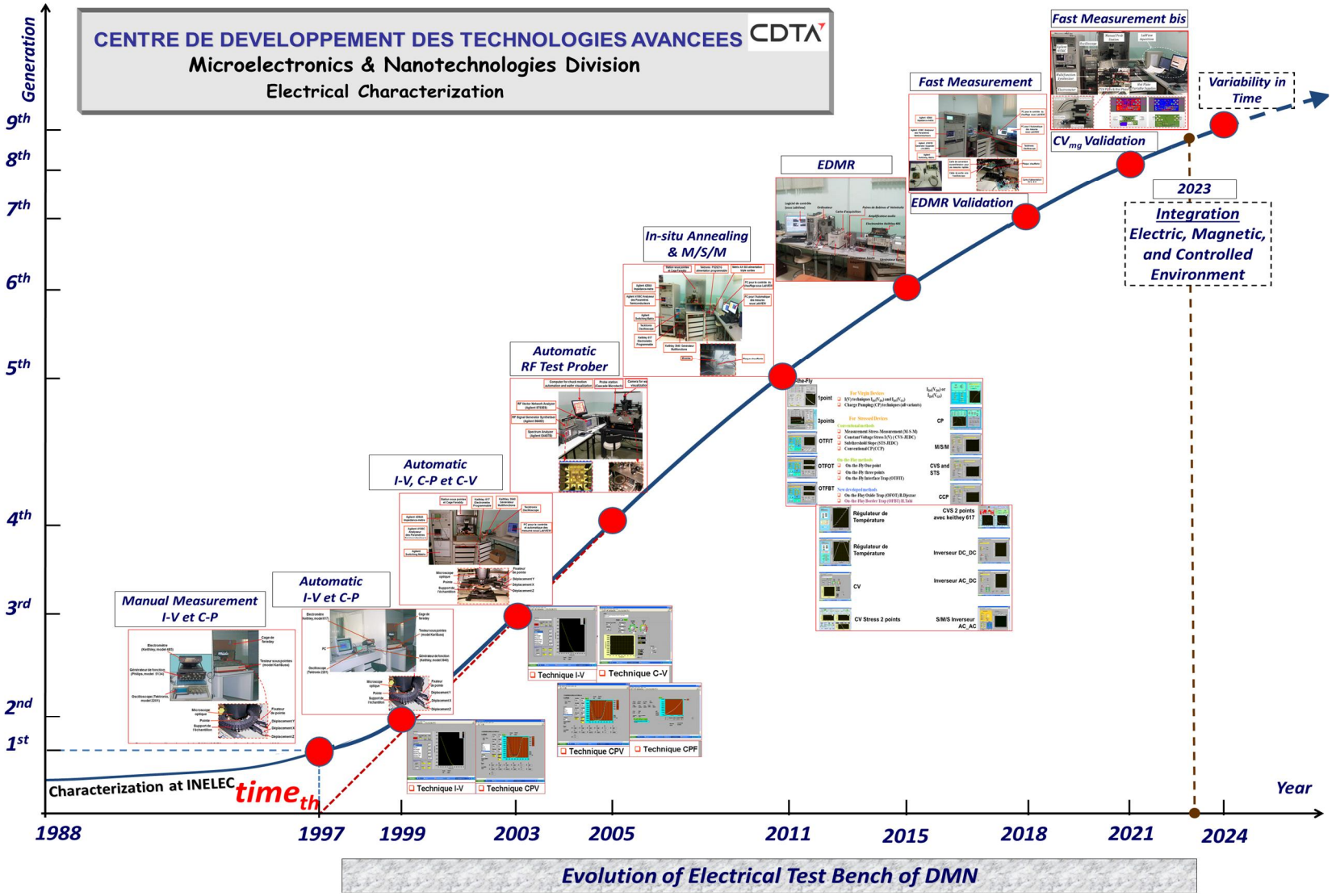

Fig. 30. Schematic illustration of the evolution of the electrical test platform, summarizing different experimental setup generations.

for radio-frequency characterization and parameter extraction of MEMS devices **[161]** and ICs **[162].** The introduction of the heat system during this decade allowed experimental explorations of NBTI failure mode, which is a key reliability issue in MOS devices **[163]**. We provided thorough modelling and experimental efforts to understand the physical mechanisms of NBTI components that are behind V_{th} degradation as well as their impact on ICs by developing novel on-the-fly methods.

In the third decade (2015-2025), we upgraded our experimental setups by adding methods based on magnetic field **[164]** and fast measurement cards **[137].** The former setup permitted the investigations of microstructures of defects caused by NBTI, while the latter allowed the measurements of fast switching traps. Using these setups, we deepened our comprehension on the physical nature of defects.

As perspective, we plan to integrate magnetic field and fast measurement under controlled environment in the same experimental setup to conduct deep analysis of semiconductor reliability at front-end-of-the-line (FEOL), back-end-of-the-line (BEOL), device/circuit, wafer, and packaging levels as well as memory (conventional/emerging) reliability and failure analysis (FA).

6. Conclusion

The paper addresses the history of the electrical characterization platform of DMN/CDTA. This review is presented in three periods. In first period, experimental setup based on Keithley instruments Karl-Süss prober were basically used to extract I-V and CP characteristics of MOS devices. It was also used to study ionizing radiation effects on Si/SiO_2 system of MOS structures. In the second period, based on semi-automated Cascade prober and Agilent equipment, more advanced experimental automatic benches were achieved. They enabled, not only to extract C-V, I-V, and CP characteristics, but also to perform RF characterization of ICs and to implement new homemade electrical methods for investigating the physical mechanisms of failure modes in MOS devices, such as NBTI, HCI, and TDDB. In the third period, more sophisticated and special in-house setups were developed, like EDMR, magnetic capacitance, and fast characterizations. The former allowed the exploration of the physical microstructures of defects behind NBTI phenomenon, the latter permitted to capture a part of fast switching traps during NBTI and HCI stresses.

As future works, it is projected to build up setups integrating magnetic and rapid measures under controlled environment as well as probe cards for spatial-temporal variability analysis of electrical parameters.

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