NBTI Fast Electrical Characterization in pMOSFET Devices

Messaoud Dhia Elhak ^{(1)*}, Djezzar Boualem ⁽²⁾, Benabdelmoumene Abdelmadjid ⁽²⁾, Boubaaya Mohamed ⁽²⁾, Zatout Boumediene ⁽²⁾, Zitouni Abdelkader ⁽¹⁾

(1) Signals & Systems Laboratory (LSS), Institute of Electrical & Electronic Engineering (IGEE),
M'HamedBougara University of Boumerdes (UMBB), Boumerdes, Algeria
(2) Microelectronics and Nanotechnology Division (DMN), Centre de Développement des
Technologies, Avancées (CDTA), Algiers, Algeria
d'.messaoud@univ-boumerdes.dz

Abstract: To measure the entire characteristic of p-MOSFET, we have implemented the fast $I_{ds}-V_{gs}$ technique. The latter is used to study NBTI phenomenon with measure-stress-measure method, for electric field5MV/cm $< E_{ox} < 7.5$ MV/cm, and temperatures $27\,^{\circ}C < T_{S} < 120\,^{\circ}C$. Measurement time has reached $10\,\mu s$, and a stress-measure delay (switching time) of about a hundred of milliseconds was obtained. However, strengths and weaknesses of the implemented technique have been discussed. Furthermore, the extraction methods: transconductance (g_m) , subthreshold slope (SS), and mid-gap (MG), have been implemented and discussed as well. NBTI parameter i.e. ΔV_{th} , n, γ and E_a were extracted and compared to other results. A time exponent n of 0.149 has been touched. Activation energy $E_a = 0.039\,\mathrm{eV}$ and a field factor $\gamma = 0.41\,\mathrm{MV}$. cm^{-1} for a stress time $t_S < 10\,s$ have been obtained.

Keywords: MOSFET reliability; NBTI; $I_{ds} - V_{as}$ fast characterization; MSM method; extraction methods.

1. INTRODUCTION

Reliability in advanced Metal Oxide Semiconductor (MOS) devices is becoming a serious issue for life time of integrated circuits [1]. One of the most important problems is negative bias temperature instability in p-type MOS-Field-Effect-Transistors (p-MOSFETs) [2]. In fact, NBTI became a big concern since first discovered [3]. It grown-up dramatically with the shrinking process of MOSFET channel length [4]-[5]. Even-though new technologies have been developed as a solution e.g. high-K (HK) insulators; such as silicon oxy-nitride (SiON) and hafnium dioxide (HfO2); but the occurring[6]-[7]. concernis still models have been proposed to explain the NBTI phenomenon, such as two-stage model [7], as-grown-generation (AG) [8], and reaction diffusion (RD) [7]. Each model has its strengths and weaknesses. In addition, many measurement techniques and methods have been developed and implemented [5]-[7]-[9]-[10] to investigate NBTI-induced degradation. They are used to extract MOSFET parameters suffered from NBTI e.g. threshold voltage shift (ΔV_{th}) , mobility degradation ($\Delta\mu$), interface states (N_{it}), and oxide traps (N_{ot}) [7]-[11]-[12]-[13]-[14]-[15]-[16]-[17]-[18].

Moreover, NBTI recovery happened very fast as soon as the stress on the gate is stopped

[12]. And like the stress interruption, measurement time delay also induces recovery. This was found to be due to spontaneous recovery [7]; which is resulted from the so-called 'fast traps'. This issue is now considered as a real concern in the understanding of the NBTI mechanism. For that, researchers concentrate on new fast measurement techniques. In 2003, A. Kerber et al. [9] developed a new measurement technique to reach 100µs in measuring time t_M , this technique can be called $fastI_{ds} - V_{gs}$. In 2004 and by using inexpensive RF measurement setup, Shen et al. recorded $t_M = 1 \mu s$ [10] and moreover $t_M = 100$ ns in 2008 [19].

In this work, we implemented the fast $I_{ds} - V_{gs}$ technique. We started by the construction of the electronic card i.e. extra transimpedance. Next, low-noise experimental setup was automated using LabView software. After that, implemented the extraction methods that could be used with this technique. Finally, we discussed the implemented technique, the extraction methods and NBTI parameters. Results are presented and compared to other works.

This paper is highlighted as follows, a global introduction in section I. Devices details, experimental setup, fast $I_{ds} - V_{gs}$ technique and extraction methods are presented in

section II. Experimental results are arranged in section III. Discussion is held on section III. Conclusion takes a place at section IV.

2. EXPERIMENTAL SETUP AND EXTRACTION PROCEDURES

Device details

Devices used in this experimental work were the p-type MOS transistors, fabricated at ISiT (Institute for Silicon Technology) of Fraunhofer, Germany.With gate insulator of SiO_2 and a gate thickness of $t_{ox} = 20 \ nm \ (200 \mbox{Å}).\mbox{A}$ gate capacitance $C_{ox} = 2.12 * 10^{-7} F/cm^2$, gate width $W = 1 \ \mu m$, and gate length $L = 0.8 \ \mu m$.

Circuit design and implementation

The idea is to measure I_d then convert it into V_{out} using (1) to be recorded by an oscilloscope using a low noise transimpedance Op-Amp. So, based on the IMEC developed pulsed $I_{ds}-V_{gs}$ method [9], and by following the procedures elaborated by Chen et al [10]-[19], we implemented this technique using the low noise Op-Amp OPA657 (bandwidth = 1.6GHz), for small signal measurements i.e. $I_d=10^{-6}~\mu\mathrm{A}$.

$$I_d = \frac{(V_{out} - V_d)}{R_d} \tag{1}$$

where, V_d is the drain voltage; $R_d = R_f + R_{in}$, plus to that, R_d contains other resistance effects like cable resistance (neglected), and the contact resistance between probes and DUT pads. Because of these resistances, calibration is needed later on data processing. However, the other resistors and capacitors shown in the circuit (Fig. 1) were added for stability enhancement. A picture of the two implemented transimpedance circuits is presented in Fig. 2.

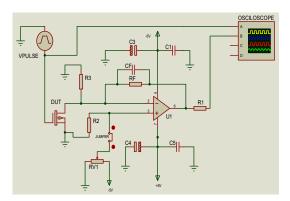


Fig.1 The circuit of the transimpedance using OPA657.



Fig.2 A picture of the implemented transimpedance.

Measurement setup

We went through three different setups to obtain the experimental setup illustrated in Fig. 3. The objective was to reach; easy manipulation, less measuring time and a wanted stress voltage. The setups were:

- MSM using Keithley 3940 for both phases (stress/measure). But we have faced a problem with output voltage limitation, 10V as maximum. This was not enough for NBTI study.
- As a solution for this problem, we have added the Keithley 617 for stress as a source with a maximum voltage of 30V, but it is still suffering from the switching time.
- To fix that, we have used the Agilent 16440A (Generator selector) as a fast switch, of course using the Agilent 4156A (SMUs) for stress and the Keithley 3940 to generate measurement signals.

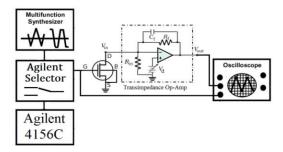


Fig.3Schematic block diagram of the fast $I_{ds} - V_{gs}$ experimental setup.

So, as a final setup, Agilent selector 16440A was used to balance between the two phases (measure/stress). Agilent 4156C for stress signals, the multifunction synthesizer Keithley 3940 to perform the measurement pulses, and the oscilloscope Tektronix Model TDS 3054B to measure the Op-Amp's output voltage. Finally, the acquisition was performed using LabView software via GPIB buses. A picture of the final measurement setup is shown in Fig. 4.



Fig.4 A picture of the experimental setup.

Measurements protocol

As a measurement protocol (see Fig. 5), DUTs were stressed logarithmically i.e. stress time t_S (2s, 4s, 6s, 8s, 10s, 20 ... 100, 200, 300s, 400s,1000s); with $V_g = V_{g,Stress}$ for 19 min; under different stress fields (5MV/cm < $E_{ox} < 7.5$ MV/cm with 0.5MV/cm increment) and different temperatures ($T_S = 27.80,100,120$ °C). The measurement pulses (could be labeled as double I_{ds}/V_{gs}) were taken at $V_g = V_{g,Measure}$ with a measurement time $t_M = 10 \, \mu s$ ($t_M = 100 \, kHz$).

Extraction Methods

Here we give an overview of the extraction methods that can be used with fast $I_{ds}-V_{gs}$ characterization, to extract NBTI-induced parameter degradation. However, some of these methods couldn't be implemented with our experimental data. The reasons behind this issue will be discussed in section III.

A. Transconductance

method (g_m) :Transconductance method [13]-[17]-[20] gives the threshold voltage more precisely comparing with CC method [12]-[13]-[16]. As shown in Fig. 6 and after calculating the transconductance

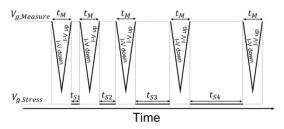


Fig.5 Fast MSM protocol used in this work.

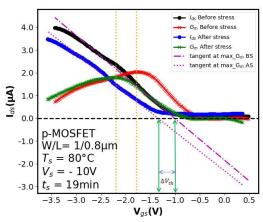


Fig.6 The I_D-V_G transfer characteristics and G_m curves for (before/after) NBTI conditions; for p-MOSFET device ($W_m=1\mu m,\ L_m=0.8\mu m$ and $t_{ox}=20\ nm$) measured at $V_D=50\ mV$; after a stress protocol of ($T_S=80\ ^{\circ}C,\ V_S=-10\ V$ and $t_S=10\ min$); where $V_{th1}=-1.05\ V$ and $V_{th2}=-1.3\ V$.

using (2), we draw the tangent at the intersection of $g_{m,max}$ with $I_d - V_g$ curve;the intercept with V_g axis is V_{th} (3).

$$g_m = \frac{dI_d}{dV_g}\Big|_{V_d = st} \tag{2}$$

$$V_{th} = V_g \big|_{I_d = 0} \tag{3}$$

B. Subthreshold slope method (SS):Subthreshold slope method [14] uses the slope of the subthreshold region of $I_d - V_g$, as shown in Fig. 7. It gives the shift of both interface state density ΔN_{it} (4) and trapped oxide charge density ΔN_{ot} (5).

$$\Delta N_{it} = \Delta S \frac{C_{ox} \ln{(\frac{N_{a,d}}{n_i})}}{q \ln{(10)}}$$
 (4)

$$\Delta N_{ot} = (\Delta S - \Delta V_{th}) \frac{C_{ox}}{q}$$
 (5)

and

$$\Delta S = \frac{1}{s_2} - \frac{1}{s_1} \tag{6}$$

where, $N_{a,d}$ is the channel doping (cm^{-3}) . s_1 and s_2 are the subthreshold slopes measured before and after stress, respectively.

C. Mid-Gap method (*MG*):Assuming that interface traps N_{it} are not involved in ΔV_{th} when Fermi level is at the mid-gap (MG), the bands are bent at the interface inducing

current flow of amount $(\phi_b=kT/q)\ln{(N_a/n_i)}$. $I_{mg}=10^{-14}A$ atroom temperature. So at MG level, $\Delta V_{th}=\Delta V_{mg}=\Delta V_{ot}$). [11]-[14]-[15]

$$\Delta V_{th} = \Delta V_{N_{it}} + \Delta V_{N_{ot}} \tag{7}$$

$$\Delta V_{N_{ot}} = \Delta V_{mg} = V_{mg2} - V_{mg1} \qquad (8)$$

$$\Delta N_{ot} = \Delta V_{N_{ot}} \frac{C_{ox}}{a} \tag{9}$$

$$\Delta N_{it} = \Delta V_{N_{it}} \frac{C_{ox}}{a} \tag{10}$$

where, $\Delta V_{N_{it}}$ and $\Delta V_{N_{ot}}$ are the voltage shifts induced by interface traps and oxide traps, respectively. V_{mg2} and V_{mg1} are the mid-gap voltages before and after stress, respectively. The method is presented in Fig. 7.

D. n, γ and E_a extraction method: From RD model point of view [7], we convert (11) into logarithmic scale, as shown in (12). After that we fit the threshold voltage shift versus stress time (t) to get the power exponent n, as given by (13); versus stress field (E_{ox}) to get the acceleration factor γ (see (14)); and versus stress temperature (T) to get the activation energy E_a (15).

$$\Delta V_{th} = A \exp(\gamma E_{ox}) \exp\left(\frac{-E_a}{kT}\right) t^n$$
 (11)

$$\log (\Delta V_{th}) = \log(A) + \frac{\gamma E_{ox} - E_a}{kT} + nlog(t)$$
(12)

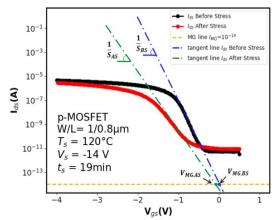


Fig.7 Presentation of both SS method and MG method for (before/after) NBTI; on p-MOSFET device ($W_m=1\mu m,\ L_m=0.8\mu m\ and\ t_{ox}=20\ nm$) measured at $V_D=50\,\mathrm{mV}$; after a stress protocol of ($T_S=120\,^{\circ}C,\ V_S=-14\ V\ and\ t_S=19\ min$).

$$n = d\log \left(\Delta V_{th}\right) / d\log \left(t\right)|_{A, E_{ox}, T = st}$$
 (13)

$$\gamma = d\log \left(\Delta V_{th}\right) / dE_{ox}|_{A,t,T=st}$$
 (14)

$$E_a = d\log (\Delta V_{th})/d(1/kT)|_{A,t,E_{\alpha r} = st}$$
 (15)

3. EXPERIMENTAL RESULTS

Data analysis as a final phase in the experimental work was an important phase. For that, calibration, smoothing, extraction implementation methods and figures visualization were performed using Python software. Fig. 8 presents the smoothing process of the collected data. As shown in the figure, data were not ready to use (extraction & interpretation) i.e. so noisy. We went through two smoothing processes; normal average filtering and polynomial fitting. For I_{on} (device on) interpretation average filtering was extremely enough. However, when it comes to I_{off} (device off) polynomial fitting proved its competence in front of the first one. Using the polynomial fitting, allows us to easily investigate what happened on that spot i.e. I_{off} , as we will see later. Extraction methods g_m , SS, and MGwere shown previously in Fig. 6 and Fig. 7, respectively. Despite SS and MG methods couldn't be used with fast $I_d - V_g$, but they were implemented to extract ΔV_{it} and ΔV_{ot} conventional $I_d - V_g$. Fig. presents ΔV_{it} (extracted using SS) and ΔV_{ot} (extracted using MG) versus E_{ox} , for the same device and under the same conditions.

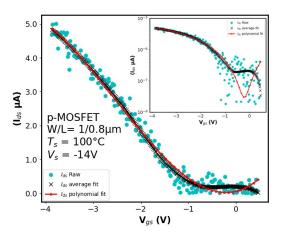


Fig.8Filtering process on p-MOSFET device $(W_m=1\mu m,\ L_m=0.8\mu m \ {\rm and}\ t_{ox}=20\ nm)$ after a stress protocol of $(T_S=100\ {}^{\circ}\text{C},\ V_S=-14\ V \ {\rm and}\ t_S=19\ min)$.

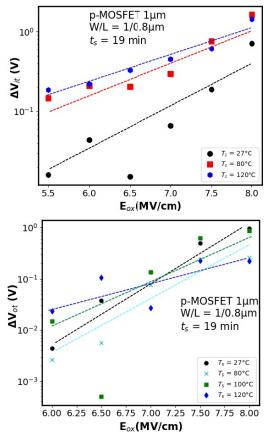


Fig.9 Extracted ΔV_{it} and ΔV_{ot} from p-MOSFET device of $0.18\mu m$ technology with $(W_m=1\mu m,L_m=0.8\mu m$ and $t_{ox}=20~nm$); On the top ΔV_{it} shift versus E_{ox} for a stress duration of $t_s=19~min$ extracted using SS method, and on the bottom ΔV_{ot} shift versus E_{ox} for a stress duration of $t_s=19~min$ extracted using MG method.

Fig. 10 presents the MSM results using both classical and fast I_d-V_g characterizations. Both techniques show NBTI time dependency in p-type MOSFET devices. It is very clear that fast $I_{ds}-V_{gs}$ characterization allows us to investigate smaller time intervals comparing to the classical one.

Plus, the new technique proved that NBTI depends strongly on the stress time. It can be seen clearly that, the more the stress the more the resulted threshold voltage shift ΔV_{th} and the less in the on-current of the $deviceI_{on}$. However, the latter deteriorates because of mobility (μ/μ_0) degradations. Here, we can say that; besides the temperature dependency of the cut-off current, NBTI stress field provides leakage current in p-MOSFET devices as well.On the other hand, Fig. 11 presents interface states degradation (ΔN_{it}) as a function of time for different stress fields. These measures resulted from a MSM protocol of 1h (3600s), with stress time $t_s = 100s$ before

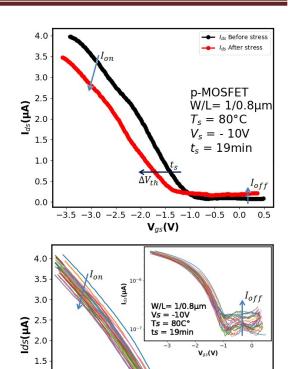


Fig.10Classical I_d-V_g characteristic (top) and fast I_d-V_g characteristic (bottom) curves as a function of stress time (t_s) under NBTI conditions $(T_s=80~^{\circ}C,~V_s=-10~V~and~t_s=19~min);$ on p-MOSFET device $(W_m=1\mu m,~L_m=0.8\mu m~andt_{ox}=20~nm$) measured at $V_D=50$ mV.

Vgs(V)

-2.0

1.0 W/L= 1/0.8μm

Vs = -10V

 $Ts = 80C^{\circ}$

 $_{0.0}$ ts = 19min

0.5

each measure. The implemented technique was the regular $I_d - V_g$ characterization, using Agilent 4156C. It is clear that the regular technique shows the dependency with a time exponent0.149 < n < 0.33. But, this time exponent is not clear at the first stage; the one labeled 'fast degradation'. In fact, it shows a jump instead; at this level this jump couldn't be interpreted $(n \gg 1)$. Now, for that and also to avoid NBTI degradation recovery, fast $I_{ds} - V_{as}$ characterization was proposed.

Now, using this technique, gives the hand to investigate NBTI degradation in small stress durations i.e. $t_s \ll 10^2 s$. Furthermore, with this technique our measurement is almost out of recovery i.e. I_{ds} characteristic is taken in less than 10 µs; 100 ns elsewhere [19]. Fig. 12 shows NBTI time dependence with a time exponent 0.149 < n < 0.33, these results are similar to others [21]-[22]. In addition to time dependency, NBTI shows other dependencies; electric field and temperature.

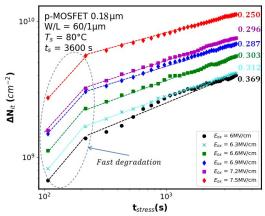


Fig.11 ΔN_{it} shift versus time for a stress duration of $t_s=3600~s$ (measures were taken each 100~s); under stress temperature $T_s=80~^{\circ}C$; for E_{ox} from 6to 7.5MV/cm; with the presentation of n exponent; on p-MOSFET device of $0.18\mu m$ technology with ($W_m=60\mu m$, $L_m=1\mu m$ and $t_{ox}=20~nm$).

It depends strongly on the stress electric field. It can be seen clearly from Fig. 12, Fig. 13, and Fig. 14 that the more the stress, time and temperature, the more the threshold voltage shift ΔV_{th} . Even though time, field and temperature dependencies exist, but they don't follow the same mechanism. It is clear that time exponent and activation energy show a clear dependence compared to y field factor. Electric field factor γ and activation energy E_a are both extracted and plotted in Fig. 13 and Fig. 14, respectively. The extracted field factor values were found lower $(0.28 \text{ cm/MV} < \gamma < 0.61 \text{ cm/MV})$ with that given in [23]. That's return strongly to the stress time i.e. < 10s in our case, and > 100s with others [23].

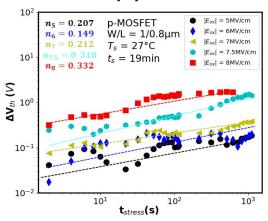


Fig.12 ΔV_{th} shift versus time for a stress duration of $t_s=19~mim$ under stress temperature $T_s=27^{\circ}C$; for different stress fields E_{ox} ; with the presentation of n exponent; on p-MOSFET device ($W_m=1\mu m$, $L_m=0.8\mu m$ and $t_{ox}=20~nm$).

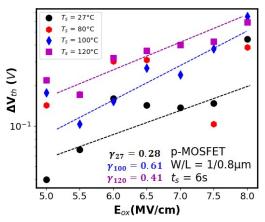


Fig.13 ΔV_{th} shift versus electric fields E_{ox} after a stress duration of $t_s=6s$; under different stress temperatures; with the presentation of the field factor γ ; on p-MOSFET ($W_m=1\mu m$, $L_m=0.8\mu m$ and $t_{ox}=20~nm$).

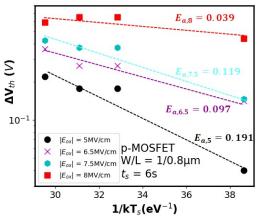


Fig.14 Threshold voltage degradation with activation energy E_a presentation as a function of temperature variation, after a stress duration of $t_s=6s$; under different stress fields; on p-MOSFET ($W_m=1\mu m$, $L_m=0.8\mu m$ and $t_{ox}=20~nm$).

For activation energies literature states that neutral H_2 diffusion is described with $0.2 \text{ eV} < E_a < 0.3 \text{ eV}$ and the time exponent $n \approx 0.25$ [5]. Moreover, recent measurements of nitride-oxides gave $0.19 \text{ eV} < E_a < 0.24 \text{ eV}$ and 0.095 < n < 0.158 over the 183 -513 °K temperature range, in contrast to the previous values, for pure $SiO_2[5]$ -[24]. A more commonly-accepted value for dry SiO₂ is 1 - 0.15 eV. The value of 0.27 eV is likely due to partial wet oxide. Or, it is due to different defect generation mechanisms i.e. $E_a \approx 0.02 \, eV$ is referred to hole trapping while $E_a \approx 0.25 \, eV$ to hydrogen diffusion; as reported here [5]-[24]. However, our results showed a good agreement with literature; we recorded 0.039 eV $< E_a < 0.191$ eV. should mention that our devices were fabricated in dry oxidation, for that E_a is lower. Also, it can be noticed (from Fig. 14) that E_a is influenced by stress field E_{ox} i.e. it shows a concave-up at $E_{ox} = 7.5$ MV/cm.

4. DISCUSSION

proceed Before we parameters in interpretation, we should explain the appearance of different technologies in this i.e. 1 μm for fast $I_{ds} - V_{gs}$ characterization and 0.18 µm for the classical one. It is out of the paper's scope; however, the effect of this variation (i.e. gate geometry) has been discussed and modeled as well, based on CP measurements [25]. The latter modeling approach did not account for NBTI degradation; it was just expected to be a useful tool for interface-trap densities extraction. Moreover, it has been revealed that NBTI has more breaks out in short channel transistors comparing with those of long channel [26]. Others [16], based on CC method, found that V_{th} increases with the increase of gate length. Therefore, in addition to field, temperature and stress time; gate length also included to NBTI effect (for more details see [26]). In this work we neglect geometry effect and we concentrate only on NBTI parameters.

On the other hand, g_m gave very exact values and showed better precision comparing with CC method [12]-[13]-[16]. For SS and MG, even with calibration, the exact I_d slope couldn't be reached because of high noise at very low currents i.e. $I_d \sim \mu A$. Also, our results couldn't go under $I_d = 10^{-7} \, A$ while $I_{mg} = 10^{-1} \, A$. However, both methods were used on the conventional $I_d - V_g$ to show the variation of ΔV_{it} and ΔV_{ot} as function of E_{ox} . Plus to that, solutions for these issues (i.e. high noise and I_d can't go beyond $10^{-7} \, A$) have been proposed and they would be implemented as a next work.

Also like other works [5]-[7]-[10], our measurements proved that V_{th} degradation, which is due to both interface states (ΔN_{it}) and oxide charges ΔN_{ot} , is directly proportional to the stress time. We should remind that this dependence couldn't be observed clearly on the early stages using the classical techniques. Because the very early degradation $(t < 10^2 s)$ labeled 'fast degradation' needed to be zoomed-in. However, this has been explained by the long stress duration, for which Yang et al.[5]-[27] extended the stress measurement times from $10^{-3}s$ s to 10^2s . Also it was referred to the measurements affection by the stress-tomeasure delay [5]. And it was found that the shift measured by conventional dc measurement is only 20% of the true value, and gives a very poor estimation of the trapped charge [10].

Finally, as a solution for recovery issue injected, frequently, from stress-measure interruption delays; we propose a new technique. The technique works with same principle as the presented one. The evolution would be on the generated MSM signal. We will try to generate a one-well-studied MSM signal, for all the stress protocol. We believe strongly that this technique won't be suffering from switching delays i.e. $t_{swit} = 0 \ s$.

5. CONCLUSION

In this paper, we have used MSM method, on fast $I_{ds} - V_{gs}$ measurement technique, to investigate NBTI-induced degradation in p-MOSFET devices. Using fast measurement, we have presented and discussed different extraction methods. Also, we have extracted electrical parameters and compared to other published results. Compared to the conventional ones, the present technique has shown usefulness. However, for better understanding of basic mechanisms of NBTI phenomenon, more improvements are still needed, such as reducing the time delay between stress and measurement and the leakage current of the setup. These enhancements will be achieved by proposing a new experiment setup in future work.

Acknowledgment

This work was supported by Directorate General for Scientific Research and Technological Development/Ministry of High Education and Scientific Research of Algeria (DGRSDT/MESRS) under the National Funding of Research (FNR) contract N° 05-4/FCS/DMN/ CDTA/PT 19-21. In addition, this research work would not have been possible without the contribution of FCS team members, Microelectronics and Nanotechnology Division of CDTA, so they are gratefully acknowledged for their precious helps and discussions. This work is also done in collaboration with LSS team of IGEE (ex:INELEC), many thanks for their counsels.

References

- [1] S.-H. Lee, "Technology scaling challenges and opportunities of memory devices," in *Proc. IEEE Int. Electron Devices Meeting*, Dec. 2016, pp. 1–8.
- [2] S. Mahapatra and N. Parihar, "A review of NBTI mechanisms and models," Microelectron. Reliab., vol. 81, pp. 127–135, 2018.

- [3] Y. Miura, Y. Matukura, "Investigation of silicon-silicon dioxide interface using MOS structure"; Jpn J Appl Phys 1966;5:180.
- [4] L. Jin, M. Xu; "Effect of channel length on NBTI in sub-100nm CMOS technology"; IEEE 2008 2nd IEEE International Nanoelectronics Conference - Shanghai, China (2008.03.24-2008.03.27); pp. 597—600.
- [5] D. K. Schroder, "Negative bias temperature instability: What do we understand?"; Microelectronics Reliability 47 (2007) 841– 852.
- [6] N. Kimizuka, K. Yamaguchi, K. Iniai, T. Iizuka, C. T. Liu, R. C. Keller, and T. Horiuchi, "NBTI enhancement by nitrogen incorporation into ultrathin gate oxide for 0.10-pm gate CMOS generation"; VLSI Symp. Tech. Dig., 2000, pp. 92–93.
- [7] J H. Stathis, S. Mahapatra, T. Grasser; "Controversial issues in negative bias temperature instability"; Microelectronics Reliability 81 (2018) 244–251.
- [8] B. Djezzar, A. Benabdelmoumene, B. Zatout, D. Messaoud, A. Chenouf, H. Tahi, M. Boubaaya, H. Timlelt; "Recovery investigation of NBTI-induced traps in n-MOSFET devices"; Microelectronics Reliability 110 (2020) 113703.
- [9] A. Kerber, E. Cartier, L. A. Ragnarsson, M. Rosmeulen, L. Pantisano, R. Degraeve, T. Kauerauf, G. Groeseneken, H. E. Maes, and U. Schwalke, "Characterization of the VT instability in SiO2/HfO2 gate dielectrics"; Proc. Int. Rel. Phys. Symp., 2003, p. 41.
- [10] C. Shen, M.-F. Li, X. P. Wang, Y.-C. Yeo, and D.-L. Kwong, "A fast measurement technique of MOSFET Id-Vg characteristics," IEEE Electron Device Lett., vol. 27, no. 1, pp. 55–57, Jan. 2006.
- [11] S. Winokur, J. R. Schwank, P. J. McWhorter, P. V. Dressendorfer, and D. C. Turpin, "Correlating the radiation response of MOS capacitors and transistors," IEEE Trans. Nucl. Sci., vol. NS-31, no. 6, pp. 1453–1460, Dec. 1984.
- [12] A. Bazigos, M. Bucher, J. Assenmacher, S. Decker, W. Grabinski, Y. Papananos; "An Adjusted Constant-Current Method to Determine Saturated and Linear Mode Threshold Voltage of MOSFETs"; IEEE Trans Elec Dev, Vol. 58, No. 11, Nov 2011.
- [13] A. Ortiz-Conde, F.J. Garcia S_anchez, J.J. Liou, A. Cerdeira, M. Estrada, Y. Yue; "A review of recent MOSFET threshold voltage extraction methods"; Microelectronics Reliability 42 (2002) 583–596.
- [14] B. Djezzar, H. Tahi, and A. Mokrani; "Why Is Oxide-Trap Charge-Pumping Method Appropriate for Radiation-Induced Trap Depiction in MOSFET?"; IEEE Trans (TDMR), Vol. 9, No. 2, June 2009.
- [15] P. J. McWhorter and P. S. Winokur, "Simple technique for separating the effects of interface traps and trapped-oxide charge in metal-oxide-semiconductor transistors"; Appl. Phys. Lett., vol. 48, no. 2, pp. 133–135, Jun. 1986.

- [16] X. Zhou, K.Y. Lim, W. Qian, "Threshold voltage definition and extraction for deepsubmicron MOSFETs," Solid-State Electronics, vol. 45, pp. 507-510, 2001.
- [17] Hs. Wong, H. White, J. Krutsick, V. Booth; "modeling of transconductance degradation and extraction of threshold voltage in thin oxide mosfet's"; Solid-Stare Electronics Vol. 30, No. 9, pp. 953-968. 1987.
- [19] MF. Li, D. Huang, C. Shen, "Understand NBTI Mechanism by Developing Novel Measurement Techniques"; IEEE Trans Dev Mater Rel, Vol. 8, NO. 1, Mar 2008.
- [20] T. Rudenko, V. Kilchytska, M. Khairuddin M. Arshad, JP. Raskin, A. Nazarov, and D. Flandre; "On the MOSFET Threshold Voltage Extraction by Transconductance and Transconductance-to-Current Ratio Change Methods: Part I—Effect of Gate-Voltage-Dependent Mobility"; IEEE Trans Elec Dev (TED), Vol. 58, NO. 12, Dec 2011.
- [21] D. Varghese, D. Saha, S. Mahapatra, K. Ahmed, F. Nouri, A. Alam; "On the dispersive versus Arrhenius temperature activation of NBTI time evolution in plasma nitrided gate oxides: measurements, theory, and implications"; IEEE Int Electron Dev Meet 2005:684–7.
- [22] AT. Krishnan, S. Chakravarthi, P. Nicollian, V. Reddy, S. Krishnan; "Negative bias temperature instability mechanism: the role of molecular hydrogen"; Appl Phys Lett 2006; 88:153518-1–8-3.
- [23] A. Benabdelmoumene, B. Djezzar, A. Chenouf, B. Zatout, M. Kechouane; "Analysis of NBTI Degradation in nMOS Capacitors and nMOSFETs"; IEEE Trans Dev Micro Rel (TDMR), VOL. 18, NO. 4, DECEMBER 2018.
- [24] DS. Ang, S. Wang; "On the non-Arrhenius behavior of negative-bias temperature instability"; Appl Phys Lett 2006; 88: 093506-1–6-3.
- [25] B. Djezzar, H. Tahi, A. Benabdelmoumen; "Geometric-Component Modeling in Charge-Pumping Technique"; IEEE International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA 2011) -Incheon, Korea (South) (2011.07.4-2011.07.7).
- [26] B. Djezzar, H. Tahi, A. Benabdelmoumene, A. Chenouf; "A propagation concept of negative bias temperature instability along the channel length in p-type metal oxide field effect transistor"; Solid-State Electronics 82 (2013) 46–53.
- [27] JB. Yang, TP. Chen, SS. Tan, L. Chan, "Analytical reaction-diffusion model and the modeling of nitrogen-enhanced negative bias temperature instability"; Appl Phys Lett 2006; 88:172109-1-9-3.